Silicon as a Mechanical Material

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Abstract—Single-crystal silicon is being increasingly employed in a variety of new commercial products not because of its well-established electronic properties, but rather because of its excellent mechanical properties. In addition, recent trends in the engineering literature indicate a growing interest in the use of silicon as a mechanical material with the ultimate goal of developing a broad range of inexpensive, batch-fabricated, high-performance sensors and transducers which are easily interfaced with the rapidly proliferating microprocessor. This review describes the advantages of employing silicon as a mechanical material, the relevant mechanical characteristics of silicon, and the processing techniques which are specific to micromechanical structures. Finally, the potentials of this new technology are illustrated by numerous detailed examples from the literature. It is clear that silicon will continue to be aggressively exploited in a wide variety of mechanical applications complementary to its traditional role as an electronic material. Furthermore, these multidisciplinary uses of silicon will significantly alter the way we think about all types of miniature mechanical devices and components.

I. Introduction

IN THE SAME WAY that silicon has already revolutionized the way we think about electronics, this versatile material is now in the process of altering conventional perceptions of miniature mechanical devices and components [1]. At least eight firms now manufacture and/or market silicon-based pressure transducers [2] (first manufactured commercially over 10 years ago), some with active devices or entire circuits integrated on the same silicon chip and some rated up to 10 000 psi. Texas Instruments has been marketing a thermal point head [3] in several computer terminal and plotter products in which the active printing element abrasively contacting the paper is a silicon integrated circuit chip. The crucial detector component of a high-bandwidth frequency synthesizer sold by Hewlett-Packard is a silicon chip [4] from which cantilever beams have been etched to provide thermally isolated regions for the diode detectors. High-precision alignment and coupling assemblies for fiber-optic communications systems are produced by Western Electric from anisotropically etched silicon chips simply because this is the only technique capable of the high accuracies required. Within IBM, ink jet nozzle arrays and charge plate assemblies etched into silicon wafers [5] have been demonstrated, again because of the high precision capabilities of silicon IC technology. These examples of silicon micromechanics are not laboratory curiosities. Most are well-established, commercial developments conceived within about the last 10 years.

The basis of micromechanics is that silicon, in conjunction with its conventional role as an electronic material, and taking advantage of an already advanced microfabrication technology, can also be exploited as a high-precision high-strength high-reliability mechanical material, especially applicable wherever miniaturized mechanical devices and components must be integrated or interfaced with electronics such as the examples given above.

The continuing development of silicon micromechanical applications is only one aspect of the current technical drive toward miniaturization which is being pursued over a wide front in many diverse engineering disciplines. Certainly silicon microelectronics continues to be the most obvious success in the ongoing pursuit of miniaturization. Four factors have played crucial roles in this phenomenal success story: 1) the active material, silicon, is abundant, inexpensive, and can now be produced and processed controllably to unparalleled standards of purity and perfection; 2) silicon processing itself is based on very thin deposited films which are highly amenable to miniaturization; 3) definition and reproduction of the device shapes and patterns are performed using photographic techniques which have also, historically, been capable of high precision and amenable to miniaturization; finally, and most important of all from a commercial and practical point of view, 4) silicon microelectronic circuits are batch-fabricated. The unit of production for integrated circuits—the wafer—is not *one* individual saleable item, but contains hundreds of identical chips. If this were not the case, we could certainly never afford to install microprocessors in watches or microwave ovens.

It is becoming clear that these same four factors which have been responsible for the rise of the silicon microelectronics industry can be exploited in the design and manufacture of a wide spectrum of miniature mechanical devices and components. The high purity and crystalline perfection of available silicon is expected to optimize the *mechanical* properties of devices made from silicon in the same way that *electronic* properties have been optimized to increase the performance, reliability, and reproducibility of device characteristics. Thin-film and photolithographic fabrication procedures make it possible to realize a great variety of extremely small, high-precision mechanical structures using the same processes that have been developed for electronic circuits. High-volume batch-fabrication techniques can be utilized in the manufacture of complex, miniaturized mechanical components which may not be possible by any other methods. And, finally, new concepts in hybrid device design and broad new areas of application, such as integrated sensors [6], [7] and silicon heads (for printing and data storage), are now feasible as a result of the unique and intimate integration of mechanical and electronic devices which is readily accomplished with the fabrication methods we will be discussing here.

While the applications are diverse, with significant potential impact in several areas, the broad multidisciplinary aspects of silicon micromechanics also cause problems. On the one hand, the materials, processes, and fabrication technologies are all taken from the semiconductor industry. On the other hand, the applications are primarily in the areas of mechanical en-

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TABLE I

	Yield Strength (10^{10} dyne/cm^2)	Knoop Hardness (kg/mm^2)	Young's Modulus (10^{12} dyne/cm^2)	Density (gr/cm^3)	Thermal Conductivity (W/cm°C)	Thermal Expansion (10^{-6}/°C)
*Diamond	53	7000	10.35	3.5	20	1.0
*SiC	21	2480	7.0	3.2	3.5	3.3
*TiC	20	2470	4.97	4.9	3.3	6.4
*Al_2O_3	15.4	2100	5.3	4.0	0.5	5.4
*Si_3N_4	14	3486	3.85	3.1	0.19	0.8
*Iron	12.6	400	1.96	7.8	0.803	12
SiO_2 (fibers)	8.4	820	0.73	2.5	0.014	0.55
*Si	7.0	850	1.9	2.3	1.57	2.33
Steel (max. strength)	4.2	1500	2.1	7.9	0.97	12
W	4.0	485	4.1	19.3	1.78	4.5
Stainless Steel	2.1	660	2.0	7.9	0.329	17.3
Mo	2.1	275	3.43	10.3	1.38	5.0
Al	0.17	130	0.70	2.7	2.36	25

*Single crystal. See Refs. 8, 9, 10, 11, 141, 163, 166.

gineering and design. Although these two technical fields are now widely divergent with limited opportunities for communication and technical interaction, widespread, practical exploitation of the new micromechanics technology in the coming years will necessitate an intimate collaboration between workers in *both* mechanical *and* integrated circuit engineering disciplines. The purpose of this paper, then, is to expand the lines of communication by reviewing the area of silicon micromechanics and exposing a large spectrum of the electrical engineering community to its capabilities.

In the following section, some of the relevant mechanical aspects of silicon will be discussed and compared to other more typical mechanical engineering materials. Section III describes the major "micromachining" techniques which have been developed to form the silicon "chips" into a wide variety of mechanical structures with IC-compatible processes amenable to conventional batch-fabrication. The next four sections comprise an extensive list of both commercial and experimental devices which rely crucially on the ability to construct miniature, high-precision, high-reliability, *mechanical* structures on silicon. This list was compiled with the primary purpose of illustrating the wide range of demonstrated applications. Finally, a discussion of present and future trends will wrap things up in Section VIII. The underlying message is that silicon micromechanics is not a diverging, unrelated, or independent extension of silicon microelectronics, but rather a natural, inevitable continuation of the trend toward more complex, varied, and useful integration of devices on silicon.

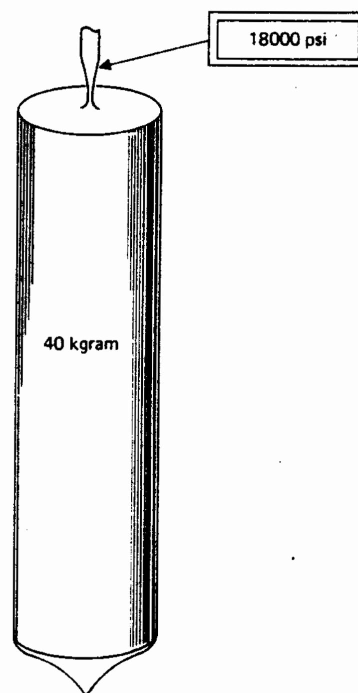


Fig. 1. Stresses encountered commonly in silicon single crystals are very high during the growth of large boules. Seed crystals, typically 0.20 cm in diameter and supporting 40-kg boules, experience stresses over 1.25×10^8 Pa or about 18 000 psi in tension.

II. Mechanical Characteristics of Silicon

Any consideration of mechanical devices made from silicon must certainly take into account the mechanical behavior and properties of single-crystal silicon (SCS). Table I presents a comparative list of its mechanical characteristics. Although SCS is a brittle material, yielding catastrophically (not unlike most oxide-based glasses) rather than deforming plastically (like most metals), it certainly is not as fragile as is often believed. The Young's modulus of silicon (1.9×10^{12} dyne/cm^2 or 27×10^6 psi) [8], for example, has a value approaching that of stainless steel, nickel, and well above that of quartz and most other borosilicate, soda-lime, and lead-alkali silicate glasses [9]. The Knoop hardness of silicon (850) is close to quartz, just below chromium (935), and almost twice as high as nickel (557), iron, and most common glasses (530) [10]. Silicon single crystals have a tensile yield strength (6.9×10^{10} dyne/cm^2 or 10^6 psi) which is at least 3 times higher than stainless-steel wire [8], [11]. In practice, tensile stresses *routinely* encountered in seed crystals during the growth of large SCS boules, for example, can be over 18 000 psi (40-kg boule hanging from a 2-mm-diameter seed crystal, as illustrated in Fig. 1). The primary difference is that silicon will yield by fracturing (at room temperature) while metals usually yield by deforming inelastically.

Despite this quantitative evidence, we might have trouble intuitively justifying the conclusion that silicon is a strong mechanical material when compared with everyday laboratory and manufacturing experience. Wafers do break—sometimes without apparent provocation; silicon wafers and parts of wafers may also easily chip. These occurrences are due to several factors which have contributed to the misconception that silicon is mechanically fragile. First, single-crystal silicon is normally obtained in large (5–13-cm-diameter) wafers, typically only 10–20 mils (250 to 500 μm) thick. Even stainless

steel of these dimensions is very easy to deform inelastically. Silicon chips with dimensions on the order of 0.6 cm × 0.6 cm, on the other hand, are relatively rugged under normal handling conditions unless scribed. Second, as a single-crystal material, silicon has a tendency to cleave along crystallographic planes, especially if edge, surface, or bulk imperfections cause stresses to concentrate and orient along cleavage planes. Slip lines and other flaws at the edges of wafers, in fact, are usually responsible for wafer breakage. In recent years, however, the semiconductor industry has attacked this yield problem by contouring the edges of wafers and by regularly using wafer edge inspection instruments, specifically designed to detect mechanical damage on wafer edges and also to assure that edges are properly contoured to avoid the effects of stress concentration. As a result of these quality control improvements, wafer breakage has been greatly reduced and the intrinsic strength of silicon is closer to being realized in practice during wafer handling. Third, chipping is also a potential problem with brittle materials such as SCS. On whole wafers, chipping occurs for the same qualitative reasons as breaking and the solutions are identical. Individual die, however, are subject to chipping as a result of saw- or scribe-induced edge damage and defects. In extreme cases, or during rough handling, such damage can also cause breakage of or cracks in individual die. Finally, the high-temperature processing and multiple thin-film depositions commonly encountered in the fabrication of IC devices unavoidably result in internal stresses which, when coupled with edge, surface, or bulk imperfections, can cause concentrated stresses and eventual fracture along cleavage planes.

These factors make it clear that although high-quality SCS is intrinsically strong, the apparent strength of a particular mechanical component or device will depend on its crystallographic orientation and geometry, the number and size of surface, edge, and bulk imperfections, and the stresses induced and accumulated during growth, polishing, and subsequent processing. When these considerations have been properly accounted for, we can hope to obtain mechanical components with strengths exceeding that of the highest strength alloy steels.

General rules to be observed in this regard, which will be restated and emphasized in the following sections, can be formulated as follows:

1) The silicon material should have the lowest possible bulk, surface, and edge crystallographic defect density to minimize potential regions of stress concentration.

2) Components which might be subjected to severe friction, abrasion, or stress should be as small as possible to minimize the total number of crystallographic defects in the mechanical structure. Those devices which are never significantly stressed or worn could be quite large; even then, however, thin silicon wafers should be mechanically supported by some technique—such as anodic bonding to glass—to suppress the shock effects encountered in normal handling and transport.

3) All mechanical processing such as sawing, grinding, scribing, and polishing should be minimized or eliminated. These operations cause edge and surface imperfections which could result in the chipping of edges, and/or internal strains subsequently leading to breakage. Many micromechanical components should preferably be separated from the wafer, for example, by etching rather than by cutting.

4) If conventional sawing, grinding, or other mechanical operations are necessary, the affected surfaces and edges should be etched afterwards to remove the highly damaged regions.

5) Since many of the structures presented below employ anisotropic etching, it often happens that sharp edges and corners are formed. These features can also cause accumulation and concentration of stress damage in certain geometries. The structure may require a subsequent isotropic etch or other smoothing methods to round such corners.

6) Tough, hard, corrosion-resistant, thin-film coatings such as CVD SiC [12] or Si_3N_4 should be applied to prevent direct mechanical contact to the silicon itself, especially in applications involving high stress and/or abrasion.

7) Low-temperature processing techniques such as high-pressure and plasma-assisted oxide growth and CVD depositions, while developed primarily for VLSI fabrication, will be just as important in applications of silicon micromechanics. High-temperature cycling invariably results in high stresses within the wafer due to the differing thermal coefficients of expansion of the various doped and deposited layers. Low-temperature processing will alleviate these thermal mismatch stresses which otherwise might lead to breakage or chipping under severe mechanical conditions.

As suggested by 6) above, many of the structural or mechanical disadvantages of SCS can be alleviated by the deposition of passivating thin films. This aspect of micromechanics imparts a great versatility to the technology. Sputtered quartz, for example, is utilized routinely by industry to passivate IC chips against airborne impurities and mild atmospheric corrosion effects. Recent advances in the CVD deposition (high-temperature pyrolytic and low-temperature RF-enhanced) of SiC [12] have produced thin films of extreme hardness, essentially zero porosity, very high chemical corrosion resistance, and superior wear resistance. Similar films are already used, for example, to protect pump and valve parts for handling corrosive liquids. As seen in Table I, Si_3N_4, an insulator which is routinely employed in IC structures, has a hardness second only to diamond and is sometimes even employed as a high-speed, rolling-contact bearing material [13], [14]. Thin films of silicon nitride will also find important uses in silicon micromechanical applications.

On the other end of the thin-film passivation spectrum, the gas-condensation technique marketed by Union Carbide for depositing the polymer parylene has been shown to produce virtually pinhole-free, low-porosity, passivating films in a high polymer form which has exceptional point, edge, and hole coverage capability [15]. Parylene has been used, for example, to coat and passivate implantable biomedical sensors and electronic instrumentation. Other techniques have been developed for the deposition of polyimide films which are already used routinely within the semiconductor industry [16] and which also exhibit superior passivating characteristics.

One excellent example of the unique qualities of silicon in the realization of high-reliability mechanical components can be found in the analysis of mechanical fatigue in SCS structures. Since the initiation of fatigue cracks occurs almost exclusively at the *surfaces* of stressed members, the rate of fatigue depends strongly on surface preparation, morphology, and defect density. In particular, structural components with highly polished surfaces have higher fatigue strengths than those with rough surface finishes as shown in Fig. 2 [17]. Passivated surfaces of polycrystalline metal alloys (to prevent intergrain diffusion of H_2O) exhibit higher fatigue strengths than unpassivated surfaces, and, for the same reasons, high water vapor content in the atmosphere during fatigue testing will significantly decrease fatigue strength. The mechanism of fatigue, as these effects illustrate, are ultimately dependent on a surface-defect-initiation process. In polycrystalline ma-

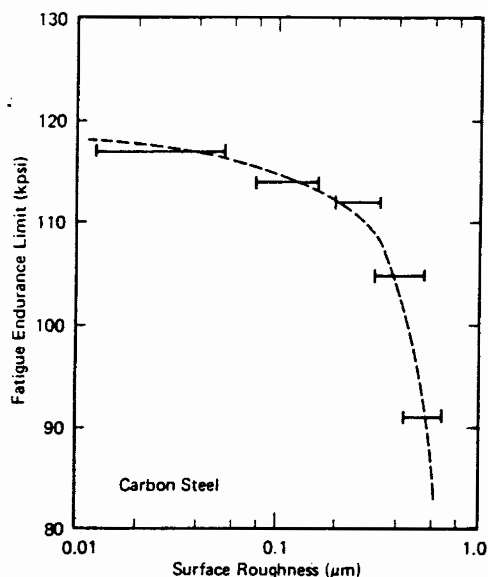


Fig. 2. Generally, mechanical qualities such as fatigue and yield strength improve dramatically with surface roughness and defect density. In the case of silicon, it is well known that the electronic and mechanical perfection of SCS surfaces has been an indispensable part of integrated circuit technology. Adapted from Van Vlack [17].

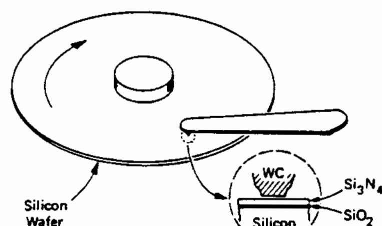


Fig. 3. A rotating MNOS disk storage device demonstrated by Iwamura *et al.* [21]. The tungsten-carbide probe is in direct contact with the nitride-coated silicon wafer as the wafer rotates at 3600 r/min. Signals have been recorded and played back on such a system at video rates. Wear of the WC probe was a more serious problem than wear of the silicon disk.

terials, these surface defects can be inclusions, grain boundaries, or surface irregularities which concentrate local stresses. It is clear that the high crystalline perfection of SCS together with the extreme smoothness and surface perfection attainable by chemical etching of silicon should yield mechanical structures with intrinsically high fatigue strengths [18]. Even greater strengths of brittle materials can be expected with additional surface treatments [9]. Since hydrostatic pressure has been shown to increase fatigue strengths [19], any film which places the silicon surface under compression should decrease the initiation probability of fatigue cracks. Si_3N_4 films, for example, tend to be under tension [20] and therefore impart a compressive stress on the underlying silicon surface. Such films may be employed to increase the fatigue strength of SCS mechanical components. In addition, the smoothness, uniformity, and high yield strength of these thin-film amorphous materials should enhance overall component reliability.

A new rotating disk storage technology which has recently been demonstrated by Iwamura *et al.* [21] not only illustrates some of the unique advantages derived from the use of silicon as a mechanical material but also indicates how well silicon, combined with wear-resistant Si_3N_4 films, can perform in demanding mechanical applications. As indicated in Fig. 3, data storage was accomplished by an MNOS charge-storage process in which a tungsten carbide probe is placed in direct contact with a 3-in-diameter silicon wafer, rotating at 3600 r/min. The wafer is coated with 2-nm SiO_2 and 49-nm Si_3N_4 while the carbide probe serves as the top metal electrode. Positive voltage pulses applied to the metal probe as the silicon passes beneath will cause electrons to tunnel through the thin SiO_2 and become trapped in the Si_3N_4 layer. The trapped charge can be detected as a change in capacitance through the same metal probe, thereby allowing the signal to be read. Iwamura *et al.* wrote and read back video signals with this device over 10^6 times with little signal degradation, at data densities as high as 2×10^6 bits/cm^2. The key problems encountered during this experiment were associated with wear of the tungsten carbide probe, not of the silicon substrate or the thin nitride layer itself. Sharply pointed probes, after scraping over the Si_3N_4 surface for a short time, were worn down to a 10-μm by 10-μm area, thereby increasing the active recording surface per bit and decreasing the achievable bit density. After extended operation, the probe continued to wear while a barely resolvable 1-nm roughness was generated in the hard silicon nitride film. Potential storage densities of 10^9 bits/cm^2 were projected if appropriate recording probes were available. Contrary to initial impressions, the rapidly rotating, harshly abraded silicon disk is not a major source of problems even in such a severely demanding mechanical application.

III. Micromechanical Processing Techniques

Etching

Even though new techniques—and novel applications of old techniques—are continually being developed for use in micromechanical structures, the most powerful and versatile processing tool continues to be etching. Chemical etchants for silicon are numerous. They can be isotropic or anisotropic, dopant dependent or not, and have varying degrees of selectivity to silicon, which determines the appropriate masking material(s). Table II gives a brief summary of the characteristics of a number of common wet silicon etches. We will not discuss plasma, reactive-ion, or sputter etching here, although these techniques may also have a substantial impact on future silicon micromechanical devices.

Three etchant systems are of particular interest due to their versatility: ethylene diamine, pyrocatechol, and water (EDP) [22]; KOH and water [23]; and HF, HNO_3, and acetic acid CH_3OOH (HNA) [24], [25]. EDP has three properties which make it indispensable for micromachining: 1) it is anisotropic, making it possible to realize unique geometries not otherwise feasible; 2) it is highly selective and can be masked by a variety of materials, e.g., SiO_2, Si_3N_4, Cr, and Au; 3) it is dopant dependent, exhibiting near zero etch rates on silicon which has been highly doped with boron [26], [27].

KOH and water is also orientation dependent and, in fact, exhibits much higher (110)-to-(111) etch rate ratios than EDP. For this reason, it is especially useful for groove etching on (110) wafers since the large differential etch ratio permits deep, high aspect ratio grooves with minimal undercutting of the masks. A disadvantage of KOH is that SiO_2 is etched at a rate which precludes its use as a mask in many applications. In structures requiring long etching times, Si_3N_4 is the preferred masking material for KOH.

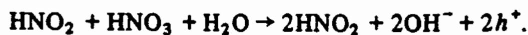
HNA is a very complex etch system with highly variable etch rates and etching characteristics dependent on the silicon dopant concentration [28], the mix ratios of the three etch

TABLE II

Etchant (Diluent)	Typical Compositions	Temp °C	Etch Rate (μm/min)	Anisotropic (100)/(111) Etch Rate Ratio	Dopant Dependence	Masking Films (etch rate of mask)	References
HF HNO_3 (water, CH_3COOH)	10 ml 30 ml 80 ml	22	0.7-3.0	1:1	$\leq 10^{17}$ cm^{-3} n or p reduces etch rate by about 150	SiO_2 (300Å/min)	24,25,28,30
	25 ml 50 ml 25 ml	22	40	1:1	no dependence	Si_3N_4	
	9 ml 75 ml 30 ml	22	7.0	1:1	-----	SiO_2 (700Å/min)	
Ethylene diamine Pyrocatechol (water)	750 ml 120 gr 100 ml	115	0.75	35:1	$\geq 7\times10^{19}$ cm^{-3} boron reduces etch rate by about 50	SiO_2 (2Å/min) Si_3N_4 (1Å/min) Au,Cr,Ag,Cu,Ta	20,26,27,35,43,44
	750 ml 120 gr 240 ml	115	1.25	35:1			
KOH (water, isopropyl)	44 gr 100 ml	85	1.4	400:1	$\geq 10^{20}$ cm^{-3} boron reduces etch rate by about 20	Si_3N_4 SiO_2 (14Å/min)	23,32,33,36,37,38,42
	50 gr 100 ml	50	1.0	400:1			
H_2N_4 (water, isopropyl)	100 ml 100 ml	100	2.0	—	no dependence	SiO_2 Al	40,41
NaOH (water)	10 gr 100 ml	65	0.25-1.0	----	$\geq 3\times10^{20}$ cm^{-3} boron reduces etch rate by about 10	Si_3N_4 SiO_2 (7Å/min)	34

mponents, and even the degree of etchant agitation, as own in Fig. 4 and Table II. Unfortunately, these mixtures n be difficult to mask, since SiO_2 is etched somewhat for all ix ratios. Although SiO_2 can be used for relatively short ching times and Si_3N_4 or Au can be used for longer times, e masking characteristics are not as desirable as EDP in icromechanical structures where very deep patterns (and erefore highly resistant masks) are required.

As described in detail by several authors, SCS etching takes ace in four basic steps [30], [31]: 1) injection of holes into e semiconductor to raise the silicon to a higher oxidation ate Si^+, 2) the attachment of hydroxyl groups OH^- to the sitively charged Si, 3) the reaction of the hydrated silicon th the complexing agent in the solution, and 4) the dissolu- n of the reacted products into the etchant solution. This ocess implies that any etching solution must provide a urce of holes as well as hydroxyl groups, and must also con- n a complexing agent whose reacted species is soluble in the chant solution. In the HNA system, both the holes and the droxyl groups are effectively supplied by the strong oxidiz- agent HNO_3, while the flourine from the HF forms the uble species H_2SiF_6. The overall reaction is autocatalytic ce the HNO_3 plus trace impurities of HNO_2 combine to m additional HNO_2 molecules.



$$HNO_2 + HNO_3 + H_2O \rightarrow 2HNO_2 + 2OH^- + 2h^+.$$

action also generates holes needed to raise the oxida- ate of the silicon as well as the additional OH^- groups cessary to oxidize the silicon. In the EDP system, ethylene mine and H_2O combine to generate the holes and the hy- xyl groups, while pyrocatechol forms the soluble species $C_6H_4O_2)_3$. Mixtures of ethylene diamine and pyrocatechol

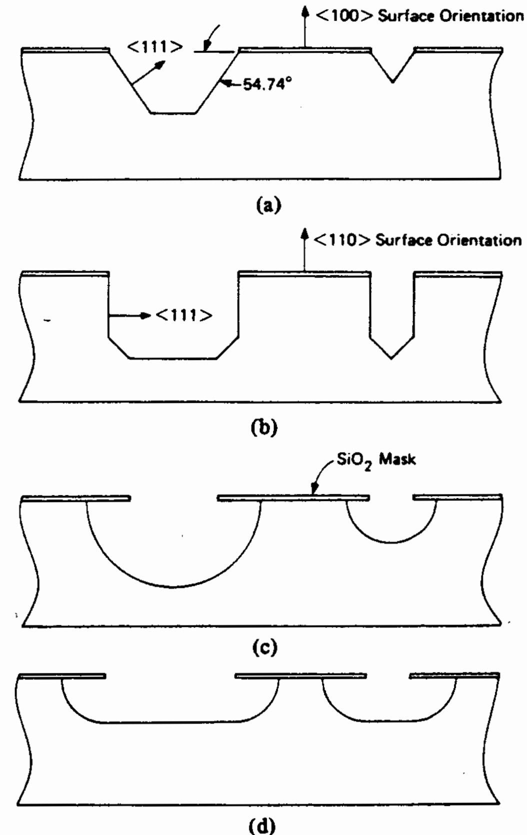


Fig. 4. A summary of wet chemically etched hole geometries which are commonly used in micromechanical devices. (a) Anisotropic etching on (100) surfaces. (b) Anisotropic etching on (110) surfaces. (c) Isotropic etching with agitation. (d) Isotropic etching without agitation. Adapted from S. Terry [29].

without water will not etch silcon. Other common silicon etchants can be analyzed in the same manner.

Since the etching process is fundamentally a charge-transfer mechanism, it is not surprising that etch rates might be dependent on dopant type and concentration. In particular, highly doped material in general might be expected to exhibit higher etch rates than lightly doped silicon simply because of the greater availability of mobile carriers. Indeed, this has been shown to occur in the HNA system (1:3:8) [28], where typical etch rates are 1-3 μm/min at p or n concentrations $>10^{18}$ cm^{-3} and essentially zero at concentrations $<10^{17}$ cm^{-3}.

Anisotropic etchants, such as EDP [26], [27] and KOH [32], on the other hand, exhibit a different preferential etching behavior which has not yet been adequately explained. Etching decreases effectively to zero in samples heavily doped with boron ($\sim 10^{20}$ cm^{-3}). The atomic concentrations at these dopant levels correspond to an average separation between boron atoms of 20-25 Å, which is also near the solid solubility limit (5×10^{19} cm^{-3}) for boron *substitutionally* introduced into the silicon lattice. Silicon doped with boron is placed under tension as the smaller boron atom enters the lattice substitutionally, thereby creating a local tensile stress field. At high boron concentrations, the tensile forces became so large that it is more energetically favorable for the excess boron (above 5×10^{19} cm^{-3}) to enter interstitial sites. Presumably, the strong B-Si bond tends to bind the lattice more rigidly, increasing the energy required to remove a silicon atom high enough to stop etching altogether. Alternatively, since this etch-stop mechanism is *not* observed in the HNA system (in which the HF component can readily dissolve B_2O_3), perhaps the boron oxides and hydroxides initially generated on the silicon surface are not soluble in the KOH and EDP etchants. In this case, high enough surface concentrations of boron, converted to boron oxides and hydroxides in an intermediate chemical reaction, would passivate the surface and prevent further dissolution of the silicon. The fact that KOH is not stopped as effectively as EDP by p^+ regions is a further indication that this may be the case since EDP etches oxides at a much slower rate than KOH. Additional experimental work along these lines will be required to fully understand the etch-stopping behavior of boron-doped silicon.

The precise mechanisms underlying the nature of chemical anisotropic (or orientation-dependent) etches are not well understood either. The principal feature of such etching behavior in silicon is that (111) surfaces are attacked at a much slower rate than all other crystallographic planes (etch-rate ratios as high as 1000 have been reported). Since (111) silicon surfaces exhibit the highest density of atoms per square centimeter, it has been inferred that this density variation is responsible for anisotropic etching behavior. In particular, the screening action of attached H_2O molecules (which is more effective at high densities, i.e., on (111) surfaces) decreases the interaction of the surface with the active molecules. This screening effect has also been used to explain the slower oxidation rate of (111) silicon wafers over (100). Another factor involved in the etch-rate differential of anisotropic etches is the energy needed to remove an atom from the surface. Since (100) surface atoms each have two dangling bonds, while (111) surfaces have only one dangling bond, (111) surfaces are again expected to etch more slowly. On the other hand, the differences in bond densities and the energies required to remove surface atoms do not differ by much more than a factor of two among the various planes, so it is difficult to use these factors alone to explain etch rate differentials in the range of several hundred or more [33] which is maintained over a relatively large temperature range. This implies that some screening effects must also play a role. It seems likely that the full explanation of anisotropic etching behavior is a combination of all these factors.

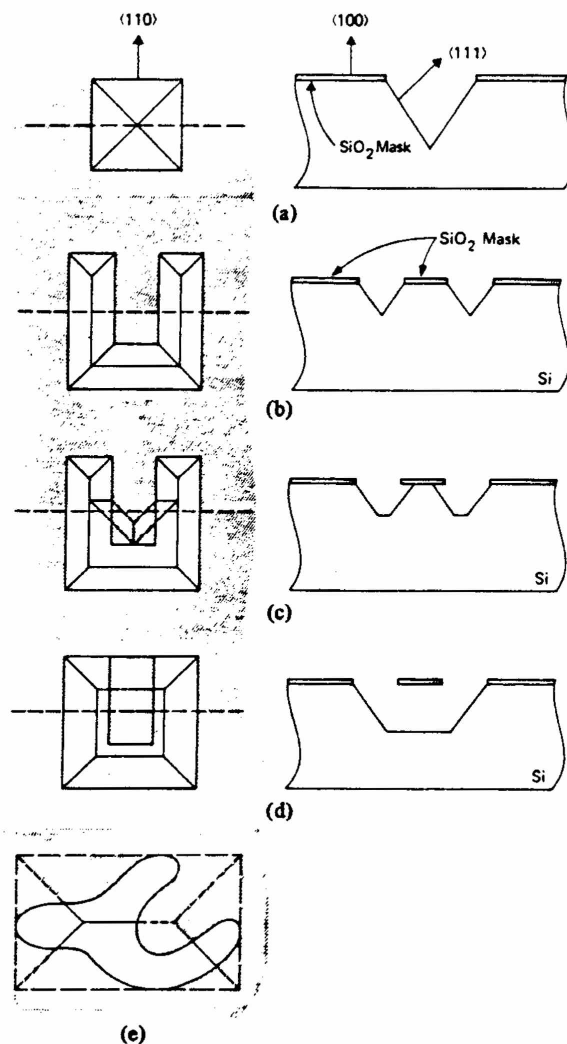


Fig. 5. (a) Typical pyramidal pit, bounded by the (111) planes, etched into (100) silicon with an anisotropic etch through a square hole in an oxide mask. (b) Type of pit which is expected from an anisotropic etch with a slow convex undercut rate. (c) The same mask pattern can result in a substantial degree of undercutting using an etchant with a fast convex undercut rate such as EDP. (d) Further etching of (c) produces a cantilever beam suspended over the pit. (e) Illustration of the general rule for anisotropic etch undercutting assuming a "sufficiently long" etching time.

Since anisotropic etching will be a particularly useful tool in the micromachining of structures described below, some detailed descriptions of the practical engineering aspects of this complex subject are deserved.

Consider a (100) oriented silicon wafer covered with SiO_2. A simple rectangular hole etched in the SiO_2 (and oriented on the surface in the (110) directions) will result in the familiar pyramidal-shaped pit shown in Fig. 5(a) when the silicon is etched with an anisotropic etchant. The pit is bounded by (111) crystallographic surfaces, which are invariably the slowes etching planes in silicon. Note that this mask pattern consists only of "concave" corners and very little undercutting of the mask will occur if it is oriented properly. Undercutting due to mask misalignment has been discussed by several workers in-

cluding Kendall [33], Pugacz-Muraszkiewicz [34], and Bassous [35]. The more complicated mask geometry shown in Fig. b) includes two convex corners. Convex corners, in general, will be undercut by anisotropic etches at a rate determined by the magnitude of the maximum etch rate, by the etch rate ratios for various crystallographic planes, and by the amount of local surface area being actively attacked. Since the openings in the mask can only support a certain flux of reactants, the net undercut etch rate can be reduced, for example, by using a mask with very narrow openings. On the other hand, the undercut etch rate can be increased by incorporating a vertical etch stop layer (such as a heavily boron-doped buried layer which will limit further downward etching); in this case, the reactant flux from the bottom of the etched pit is eventually reduced to near zero when the etch-stopping layer is exposed, so the total flux through the mask opening is maintained by an increased etch rate in the horizontal direction, i.e., an increased undercut rate.

In Fig. 5(b), the convex undercut etch rate is assumed to be slow, while in Fig. 5(c) it is assumed to be fast. Total etching time is also a factor, of course. Convex corners will continue to be undercut until, if the silicon is etched long enough, the pit eventually becomes pyramidal, bounded again by the slow etching (111) surfaces, with the undercut portions of the mask (a cantilever beam in this case) suspended over it, as shown in Fig. 5(d). As an obvious extension of these considerations [34], a general rule can be formulated which is shown graphically in Fig. 5(e). If the silicon is etched long enough, any arbitrarily shaped closed pattern in a suitable mask will result a rectangular pit in the silicon, bounded by the (111) sur- ces, oriented in the (110) directions, with dimensions such that the pattern is perfectly inscribed in the resulting rectangle.

As expected, different geometries are possible on other crystallographic orientations of silicon [35]-[38]. Fig. 4 illustrates several contours of etched holes observed with isotropic etchants as well as anisotropic etchants acting on various orientations of silicon. In particular, (110) oriented wafers will produce vertical etched surfaces with essentially no undercut when lines are properly aligned on the surface. Again, the (111) planes are the exposed vertical surfaces which resist the attack of the etchant. Long, deep, closely spaced grooves have been etched in (110) wafers as shown in Fig. 6(a). Even wafers not exactly oriented in the (110) direction will exhibit this effect. Fig. 6(b) shows grooves etched into a surface which is 10° off the (110) direction—the grooves are simply oriented 10° off normal [36]. Note also that the four vertical (111) planes on a (110) wafer are not oriented 90° with respect to each other, as shown in the plan view of Fig. 6(c).

Crystallographic facet definition can also be observed after etching (111) wafers, even though long times are required due to the slow etch rate of (111) surfaces. The periphery of a hole etched through a round mask, for example, is hexagonal, bounded on the bottom, obviously, by the (111) surface [39]. The six sidewall facets are defined by the other (111) surfaces; three slope inward toward the center of the hole and the other three slope outward. The six inward and outward sloping surfaces alternate as shown in Fig. 7.

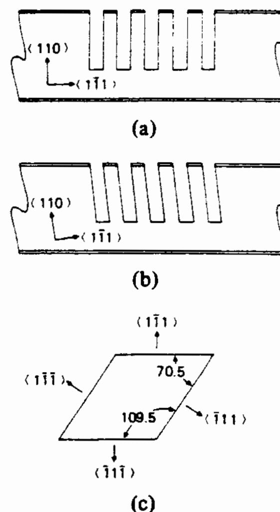


Fig. 6. Anisotropic etching of (110) wafers. (a) Closely spaced grooves on normally oriented (110) surface. (b) Closely spaced grooves on misoriented wafer. (c) These are the orientations of the (111) planes looking down on a (110) wafer.

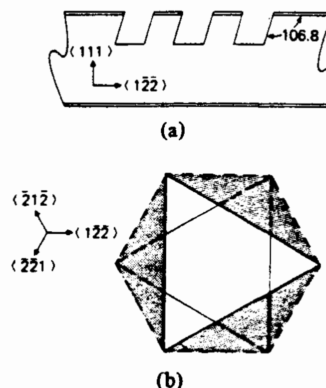


Fig. 7. Anisotropic etching of (111) silicon surfaces. (a) Wafer cross section with the steep sidewalls which would be found from grooves aligned along the (122) direction. (b) Top view of a hole etched in the (111) surface with three inward sloping and three undercut sidewalls, all (111) crystallographic planes.

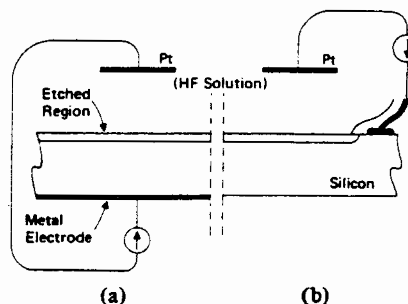


Fig. 8. Uniform electrochemical etching of wafer surfaces has been practiced in the past by making electrical contact either to the back (a) or to the front (b) of the wafer (with suitable protection for the current carrying leads). A positive voltage applied to the silicon causes an accumulation of holes at the silicon/solution interface and etching occurs. A negatively biased platinum electrode in the HF-based solution completes the circuit.

Electrochemical Etching

While electrochemical etching (ECE) of silicon has been studied and basically understood for a number of years [45]-[47], practical applications of the technique have not yet been fully realized. At least part of the reason ECE is not now a popular etching procedure is due to the fact that previous implementations of ECE offered no real advantage over the conventional, isotropic, dopant-dependent formulations discussed in the preceding section. As shown by Fig. 8(a) and (b), in typical ECE experiments electrical contact is made to the front or back of the wafer (the contacted region suitably protected from the etching solution, e.g., with wax or a special

holding fixture) and the wafer is either totally immersed or is slowly lowered into the solution while a constant current flows between the positively biased silicon electrode and the negative platinum electrode. Since etching is still, principally, a matter of charge transfer, the fundamental steps are the same as discussed above. The etchants employed, however, are typically HF/H_2O solutions. Since H_2O is not as strong an oxidizing agent as HNO_3, very little silicon etching occurs (<1 Å/min) when the current flow is zero. Oxidation, then, is promoted by applying a positive voltage to the silicon which causes an accumulation of holes in the silicon at the Si/solution interface resulting in an accumulation of OH^- in the solution at the interface. Under these conditions, oxidation of the silicon surface proceeds very rapidly while the oxide is readily dissolved by the HF. Holes, which are transported to the negative platinum electrode (cathode) as H^+ ions, are released there in the form of hydrogen gas bubbles. In addition, excess hole-electron pairs can be created at the silicon surface by optical excitation, thereby increasing the etch rate.

Since the oxidation rate is controlled by current flow and optical effects, it is again clear that the etching characteristics will depend not only on dopant type and resistivity but also on the arrangement of p and n layers in the wafer interior. In particular, ECE has been employed successfully to remove heavily doped substrates (through which large currents are easily conducted) leaving behind more lightly doped epi-layer membranes (which conduct smaller currents, thereby etching more slowly) in all possible dopant configurations (p on p^+, p on n^+, n on p^+, n on n^+) [48], [49].

Localized electrochemical jet etching has been used to generate small holes or thinned regions in silicon wafers. A narrow stream of etchant is incident on one side of a wafer while a potential is applied between the wafer and the liquid stream. Extremely rapid etching occurs at the point of contact due to the thorough agitation of the solution, the continual arrival of fresh solution at the interface, and the rapid removal of reacted products.

A more useful electrochemical procedure using an anisotropic etchant has been developed by Waggener [50] for KOH and more recently by Jackson *et al.* [51] for EDP. Instead of relying on the electric current flowing through the solution to actively etch the silicon, a voltage bias on an n-type epitaxial layer is employed to stop the dissolution of the p-type silicon substrate at the n-type epitaxial layer. This technique has the advantage of retaining all the anisotropic etching characteristics of KOH and EDP without the need for a buried p^+ layer. Such p^+ films, while serving as simple and effective etch-stop layers, can also introduce undesirable mechanical strains in the remaining membrane which would not be present in the electrochemically stopped, uniformly doped membrane.

When ECE is performed at very low current densities, or in etchant solutions highly deficient in OH^- (such as concentrated 48-percent HF), the silicon is not fully oxidized during etching and a brownish film is formed. In early ECE work, the brownish film was etched off later in a conventional HNA slow silicon etch, or the ECE solution was modified with H_2SO_4 to minimize its formation [47]. This film has since been identified as single-crystal silicon permeated with a dense network of very fine holes or channels, from much less than 1 μm to several micrometers in diameter, preferentially oriented in the direction of current flow [52], [53]. The thickness of the layer can be anywhere from micrometers up to many mils. Porous silicon, as it is called, has a number of interesting properties. Its average density decreases with increasing applied current

Fig. 9. SEM profile of laser-etched grooves [56]. The horizontal bar indicates 10 μm. Conditions were 100 torr Cl_2, 5.5-W multiline argon-ion laser, f/10 focusing, single scan at 90 μm/s. Photo courtesy of D. Ehrlich.

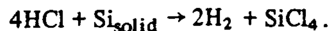
density to as low as 10 percent of normal silicon. Since it is so porous, gases readily diffuse into the structure so that the high-temperature oxidation, for example, of a relatively thick (~4-μm) porous silicon layer can be completed in a very short time (30 min at 1100°C) [52]. Several studies have been undertaken to determine the feasibility of using such deeply oxidized porous silicon regions as a planarizing, deep IC isolation technique [54]. The porous regions are defined by using Si_3N_4 masking films which are attacked relatively slowly by the concentrated HF ECE solution. Problems, however, encountered in the control and elimination of impurities trapped in the porous silicon "sponge-like" material, stress-related effects, and enhanced leakage currents in devices isolated by this technique have been difficult to overcome. Mechanical devices, on the other hand, may not be restricted by these disadvantages.

Besides magnifying the effective thermal oxidation rates, porous silicon can also be chemically attacked at enormously high rates. As expected, the interiors of the pores provide a very large surface area for exposure to the etchant solution. Wafers covered with 100-μm-thick porous silicon layer, for example, will actually shatter and explode when immersed in fast-etching HNA solutions.

Gradations in the porosity of the layer can be simply realized by changing the current with time. In particular, a low current density followed by a high current density will result in a high-porosity region covered with a low-porosity film. Since the porous region is still a single crystal covered with small holes (reported to be near 100 Å on the surface), it is not surprising that single-crystal epitaxial layers have been grown over porous silicon regions, as demonstrated by Unagami and Seki [55]. Once the thickness of the epi-layer corresponds to several times the diameter of the surface pores, it has been verified that the layer will be a uniform single crystal since the crystallinity of the substrate was maintained throughout, despite its permeation with fine holes.

A relatively new tool added to the growing list of micromechanical processing techniques is laser etching. Very high instantaneous etch rates have been observed when high-intensity lasers are focussed on a silicon surface in the presence of some gases. In particular, 20-30 MW/cm^2 of visible argon-ion laser radiation, scanned at rates of 90 μm/s in atmospheres of HCl and Cl_2 produced 3-μm-deep grooves [56], as shown in Fig. 9. At least part of the etching reaction occurs solely as a result of local thermal effects. It has been known for some time that silicon will be vigorously attacked by both these gases at temperatures above about 1000°C. Recent experi-

ments in laser annealing have verified that silicon can easily be raised above the melting point at these power densities. There is still some controversy concerning the magnitude of photochemical effects, which might aid in the dissociation of the chlorine-based molecules and enhance the etch rate. In a typical reaction, for example,



$$4HCl + Si_{solid} \rightarrow 2H_2 + SiCl_4.$$

Although many applications in the area of IC fabrication have been suggested for laser etching, the fact that the laser must be scanned over the entire wafer and the etching therefore takes place "serially," net processing time per wafer will necessarily by very high in these applications. For example, a 20-W laser at a power density of 10^7 W/cm^2 etching a 1-μm layer will require over 100 h to completely scan a 4-in-diameter wafer even if etch rates of 100 μm/s are realized. Laser etching is clearly applicable only in special micromachining processing requirements such as the various contours which may be required in print-heads, recording-heads, or other miniature mechanical structures integrated with electronics on the same silicon ship. Versatile as they are, conventional, isotropic, anisotropic, electrochemical, and ion-etching processes exhibit a limited selection of etched shapes. On the other hand, the significant key advantage of laser etching is that nearly any shape or contour can be generated with laser etching in a gaseous atmosphere simply by adjusting the local exposure dose continuously over the etched region. Such a capability will be extremely useful in the realization of complex mechanical structures in silicon.

Epitaxial Processes

While the discussion up to this point has concentrated on material removal as a micromachining technique, material addition, in the form of thin film deposition or growth, metal plating, and epitaxial growth are also important structural tools. Deposited thin films have obvious applications in passivation, wear resistance, corrosion protection, fatigue strength enhancement (elaborated on in Section II), and as very thin, high-precision spacers such as those employed in hybrid surface acoustic wave amplifiers and in other thin-film devices. On the other hand, epitaxy has the important property of maintaining the highly perfect single-crystal orientation of the substrate. This means that complex vertical and/or horizontal dopant distributions (i.e., fast and slow etching regions for subsequent micromachining by etching) can be generated over many tens of micrometers without compromising the crystal structure or obviating subsequent anisotropic processes. Etch-stop layered structures are important examples and will be considered in more detail in Section VI. Fig. 10(a), however, briefly illustrates two simple configurations: hole A is a simple etch-stop hole using anisotropic etching and a p$^+$ boron-doped buried layer while hole B is a multilevel hole in which the epilayer and a portion of the lightly doped substrate have been anisotropically etched from the edge of the p$^+$ buried region. One obvious advantage of these methods is that the depth of the hole is determined solely by the thickness of the epi-layer. This thickness can be controlled very accurately and measured even before etching begins. Such depth control is crucial in many micromechanical applications we will discuss later, particularly in fiber and integrated optics.

Where the goal of IC manufacturing is to fabricate devices as small as possible (indeed, diffusions deeper than a few micrometers are very difficult and/or time-consuming), a necessary feature of most micromechanical processing techniques is the

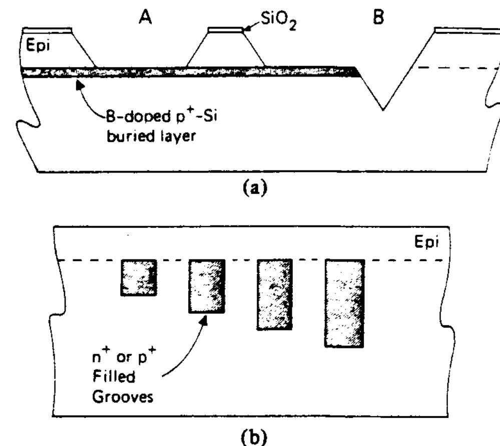


Fig. 10. (a) Since anisotropic etchants such as KOH and EDP exhibit reduced etch rates on silicon heavily doped with boron, many useful structures have been realized by growing epi over a diffused region to form a buried etch-stop layer. (b) Diagram showing how epitaxial silicon could be grown preferentially [57] in vertical-walled grooves. Doped grooves with large cross sections (>25 X 25 μm) can then be buried beneath an ordinary epi-layer.

ability to generate structures on the order of tens or even hundreds of micrometers. Both etching and epitaxial deposition possess this property. Epitaxial silicon can be grown at rates of 1 μm/min, so that layers even greater than 100 μm are readily attainable. In addition, the process parameters can be accurately controlled to allow the growth of complex three-dimensional patterns. For example, since the growth rate depends critically on temperature and gas-mixing dynamics, increased deposition rates can be observed at the *bottom* of deep, narrow, anisotropically etched grooves. In this way, Runyan *et al.* [57] (and later Smeltzer) were able to completely fill 10-μm-wide grooves (up to 100 μm deep) epitaxially with negligible silicon growth over the rest of the wafer surface. The simultaneous addition of HCl gas during the growth process is required to obtain these unusual results. Since HCl gas is an isotropic silicon etchant at these temperatures, the silicon which is epitaxially grown on the outer surface is immediately etched away in the flowing gas stream. Silicon grown in the poorly mixed atmopshere of the grooves, however, etches at a much slower rate and a net growth occurs in the groove. Heavily doped, buried regions extending over tens of micrometers are easily imagined under these circumstances as indicated in Fig. 10(b). After refilling the grooves with heavily doped silicon, the surface has been lightly etched in HCl and a lightly doped layer grown over the entire wafer. These results could not be obtained by conventional diffusion techniques. One implementation of such structures which has already been demonstrated is in the area of high-power electronic devices [58], to be discussed below in more detail. Such a process could also be used in mechanical applications to bury highly doped regions which would be selectively etched away at a later stage to form buried channels within the silicon structure.

Finally, a limited amount of work has been done on epitaxial growth through SiO_2 masks. Normally under these conditions, SCS will grow epitaxially on the bare, exposed crystal while polycrystalline silicon is deposited on the oxide. This mixed deposit has been used in audio-frequency distributed-filter, electronic circuits by Gerzberg and Meindl at Stanford [59]. At reduced temperatures, however, with HCl added to the H_2 and $SiCl_4$ in the gas stream no net deposits will occur on the SiO_2 while faceted, single-crystal, epitaxial pedestals will grow on the exposed regions since polysilicon is etched

by the HCl at a faster rate than the SCS [60]. Such epitaxial projections may find use in future three-dimensional micromechanical structures.

Thermomigration

During 1976 and 1977, Anthony and Cline of GE laboratories performed a series of experiments on the migration of liquid eutectic Al/Si alloy droplets through SCS [61]-[67]. At sufficiently high temperatures, Al, for example, will form a molten alloy with the silicon. If the silicon slice is subjected to a temperature gradient (approximately 50°C/cm, or 2.0°C across a typical wafer) the molten alloy zone will migrate toward the hotter side of the wafer. The migration process is due to the dissolution of silicon atoms on the hot side of the molten zone, transport of the atoms across the zone, and their deposition on the cold side of the zone. As the Al/Si liquid region traverses the bulk, solid silicon in this way, some aluminum also deposits along with the silicon at the colder interface. Thermomigration hereby results in a p-doped trail extending through, for example, an n-type wafer. The thermomigration rate is typically 3 μm/min at 1100°C. At that temperature, the normal diffusion rate of Al in silicon will cause a lateral spread of the p-doped region of only 3-5 μm for a migration distance of 400 μm (the full thickness of standard silicon wafers).

Exhaustive studies by Anthony and Cline have elucidated much of the physics involved in the thermomigration process including migration rate [62], p-n junction formation [64], stability of the melt [65], effect of dislocations and defects in the silicon bulk, droplet morphology, crystallographic orientation effects, stresses induced in the wafer as a result of thermomigration [67], as well as the practical aspects of accurately generating, maintaining, and characterizing the required thermal gradient across the wafer. In addition, they demonstrated lamellar devices fabricated with this concept from arrays of vertical junction solar cells, to high-voltage diodes, to negative-resistance structures. Long migrated columns were found to have smaller diameters in (100) oriented wafers, since the droplet attains a pyramidally tapered point whose sides are parallel to the (111) planes. Migrated lines with widths from 30 to 160 μm were found to be most stable and uniform in traversing 280-μm-thick (100) wafers when the lines were aligned along the (110) directions. Larger regions tended to break up into smaller independent migrating droplets, while lines narrower than about 30 μm were not uniform due to random-walk effects from the finite bulk dislocation density in the wafer. Straight-line deviations of the migrated path, as a result of random walk, could be minimized either by extremely low ($\ll 100/cm^2$) or extremely high ($>10^7/cm^2$) dislocation densities. On the other hand, the dislocation density in the recrystallized droplet trail is found to be essentially zero, not unexpected from the slow, even, liquid-phase epitaxy which occurs during droplet migration. Dopant density in the droplet trail corresponds approximately to the aluminum solid solubility in silicon at the migration temperature $\sim 2 \times 10^{19}$ cm^{-3}, which corresponds to $\rho = 0.005$ $\Omega \cdot$ cm. The p-type trail from a 50-μm-diameter aluminum droplet migrated through a 300-μm-thick n-type wafer would, therefore, exhibit less than 8-Ω resistance from front to back and would be electrically well-isolated from other nearby trails due to the formation of alternating p-n junctions, as shown in Fig. 11.

Nine potential sources of stress (generated in the wafer from the migrated regions) have been calculated by Anthony and Cline. Maximum stresses intrinsic to the process (i.e., those which are present even when processing is performed properly) are estimated to be as high as 1.39×10^9 dyne/cm^2, which can be substantially reduced by a post-migration thermal anneal. Although the annealed stress will be about two orders of magnitude below the yield point of silicon at room temperature, it may increase the susceptibility of the wafer to fracture and should be minimized, especially if a large number of migrated regions are closely spaced.

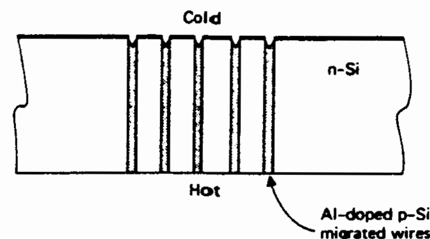


Fig. 11. In some applications of silicon micromechanics, it is important to connect the circuitry on one side of a wafer to mechanical structures on the other side. Thermomigration of Al wires, discussed extensively by Anthony and Cline [61]-[67], allows low-resistance (<8-Ω), close-spaced (<100-μm) wires to be migrated through thick (375-μm) wafers at reasonable temperatures (~1100°C) with minimal diffusion (<2 μm).

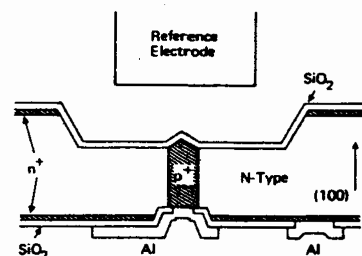


Fig. 12. Structure of the gate-controlled diode of Wen and Zemel [69]. Circuitry is on the bottom (protected) side of the wafer, while the sensor electrode is on the top. The p^+ feedthrough was accomplished by thermomigration of Al from the circuit side to the sensor side of the wafer. For ionic concentration measurements, an appropriate ion-sensitive membrane must be deposited over the oxide on the sensor side. Figure courtesy of C. C. Wen.

One obvious utilization of thermomigration is the connection of circuitry on one side of a wafer to a mechanical function on the other side. Another application may be the dopant-dependent etching of long narrow holes through silicon. Since the work of Anthony and Cline, the thermomigration process has been used to join silicon wafers [68] and to serve as feedthroughs for solid-state ionic concentration sensors (see Fig. 12) [69]. Use of thermomigrated regions in power devices is another potential application. Even more significantly, laser-driven thermomigration has been demonstrated by Kimerling *et al.* [70]. Such a process may be extremely important in practical implementations of these migration techniques, especially since the standard infrared or electron-beam heating methods used to induce migration are difficult to control uniformly over an entire wafer.

Field-Assisted Thermal Bonding

The use of silicon chips in exposed, hostile, and potentially abrasive environments will often require mounting techniques substantially different from the various IC packaging method now being utilized. First reported by Wallis and Pomerantz in 1969, field-assisted glass-metal thermal sealing [71] (sometimes called Mallory bonding after P. R. Mallory and Co., Inc., where Wallis and Pomerantz were then employed) seems to

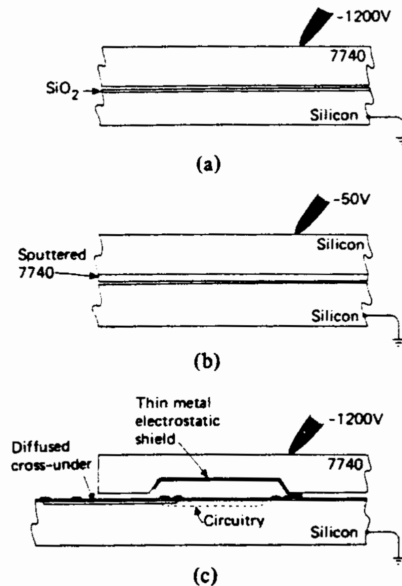


Fig. 13. Field-assisted thermal bonding can be used to hermetically bond (a) 7740 glass to silicon (bare or oxidized) or (b) silicon to silicon simply by heating the assembly to about 300°C and applying a voltage. Glass can be bonded to IC chips (c) if the circuitry is first protected by etching a shallow (~10-μm) well in the glass and depositing a grounded metal shield inside the well [76].

fulfill many of the requirements for bonding and mounting micromechanical structures. The technique is simple, low temperature, high strength, reliable, and forms hermetic seals between metals and conventional alkali-silicate glasses [72]. It is also very similar to well-known high-temperature thermal bonds where the cohesive metal–oxides, which are generated during the heating process, readily mix with the viscous glass. In the case of silicon, a glass slide is placed over a polished wafer (bare *or* thermally oxidized), the assembly is heated to about 400°C, and a high voltage (~1200 V) is applied between the silicon and the metal contact to the other side of the glass. If the sample is not too large, the metal contact may be a simple point probe located near one corner as shown in Fig. 13(a). Since the negative electrode is applied to the glass, ionic conduction causes a drift of positive ions away from the glass/Si interface into the bulk of the glass. The depletion of positive ions at the interface results in a high electric field across the air gap between the two plates. Electrostatic forces here, estimated to be higher than 350 psi, effectively clamp the pieces locally, conforming the two surfaces to obtain the strong, uniform, hermetic seal characteristic of field-assisted thermal bonding. The bonding mechanism itself has been the subject of some controversy, as discussed recently by Brownlow [73]. His convincing series of deductions, however, suggest that the commonly observed initial current peak at the onset of bonding is actually dissipated in the newly formed, narrow space-charge region in the glass at the interface. This high energy-density pulse, in the early stages of bonding, was shown to be capable of increasing the interfacial temperature by as much as 560°C, more than enough to induce the familiar, purely thermal glass/metal seal. Brownlow shows how this model correlates well with several other features observed during the bonding process.

From a device viewpoint, it is important to recognize that the relative expansion coefficients of the silicon and glass should match as closely as possible to alleviate thermal stresses after the structure has cooled. This aspect of field-assisted bonding also has the obvious advantage of yielding integrated mechanical assemblies with very small mechanical drifts due to ambient temperature variations. Corning borosilicate glasses 7740 and 7070 have both been used successfully in this regard. In addition, Brooks *et al.* [74] have even bonded two silicon wafers by sputtering approximately 4 μm of 7740 glass over one of the wafers and sealing the two as already described, with the negative electrode contacting the coated wafer as shown in Fig. 13(b). Since the glass is so thin, however, the sealing voltage was not required to be above 50 V.

A high degree of versatility makes this bonding technique useful in a wide variety of circumstances. It is not necessary to bond to bare wafers, for example; silicon passivated with thermal oxide as thick as 0.5 μm is readily and reliably bonded at somewhat higher voltage levels. The bonding surface may even be partially interrupted with aluminized lines, as shown by Roylance and Angell [75], without sacrificing the integrity or hermeticity of the seal since the aluminum also bonds thermally to the glass. In addition, glass can be bonded to silicon wafers containing electronic circuitry using the configuration shown in Fig. 13(c) [76]. The circuitry is not affected if a well is etched in the glass and positioned over the circuit prior to bonding. A metal film deposited in the well is grounded to the silicon substrate during actual bonding and serves as an electrostatic shield protecting the circuit. Applications of all these aspects will be presented and expanded upon in the following sections.

IV. Grooves and Holes

Even simple holes and grooves etched in a silicon wafer can be designed and utilized to provide solutions in unique and varied applications. One usage of etched patterns in silicon with far-reaching implications, for example, is the generation of very high precision molds for microminiature structures. Familiar, pyramidal-shaped holes anisotropically etched in (100) silicon and more complex holes anisotropically etched in (110) silicon were used by Kiewit [77] to fabricate microtools such as scribes and chisels for ruling optical gratings. After etching the holes in silicon through an SiO_2 mask, the excess SiO_2 was removed and very thick layers of nickel-phosphorus or nickel–boron alloys were deposited by electroless plating. When the silicon was completely etched away from the thick plated metal, miniature tools or arrays of tools were accurately reproduced in the metal with geometrically well-defined points having diameters as small as 50 nm. The resulting metal tools had a hardness comparable to that of file steel.

Similar principles were employed by Wise *et al.* [78] to fabricate miniature hemispherical structures for use as thermonuclear fusion targets. In these experiments, a large two-dimensional array of hemispherical holes was etched into a silicon wafer using an HNA isotropic solution, approximately as shown in Fig. 4(c). After removing the $SiO_2/Cr/Au$ etch mask, polymer, glass, metal, or other thin films are deposited over the wafer, thereby conforming to the etched hemispherical shapes. When two such wafers are aligned and bonded, the silicon mold can be removed (either destructively by etching or nondestructively by using a low adhesion coating between the silicon and the deposited film). The resulting molded shape is a thin-walled spherical shell made from the deposited material. Fig. 14 is the process schedule for a simple metal hemishell demonstrated by Wise *et al.*

The potential of making arrays of sharp points in silicon itself by etching was employed in a novel context by Thomas and Nathanson [79], [80]. They defined a very fine grid

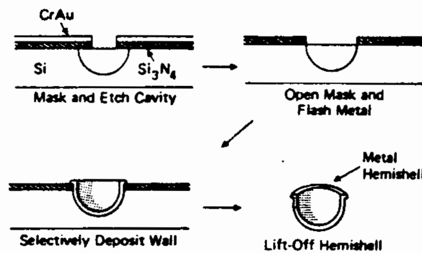


Fig. 14. Fabrication sequence for free-standing metal hemishells using an isotropic silicon-etching technique [78]. Typical dimensions of the hemishell are 350-μm diameter with a 4-μm-thick wall. Courtesy of K. D. Wise.

(typically 25 μm center to center) in an SiO_2 mask, then isotropically etched the silicon exposed in the grid lines with an HNA mixture. The isotropic etch undercuts each square segment of the oxide grid uniformly around its periphery. If the etching is quenched just after the oxide segments are completely undercut and fall from the surface, a large array of very sharply tipped silicon points is obtained. Point diameters were estimated to be about 20 nm. These silicon points, at densities up to 1.5×10^5 cm^2, were used by Thomas and Nathanson as efficient, uniform, photosensitive field emitter arrays which were imaged onto a phosphor screen closely spaced to the wafer. A more complex extension of this fabrication technique will be described below in the section on Thin Cantilever Beams.

Ink Jet Nozzles

Since anisotropic etching offers a powerful method for controlling undercutting of masks during silicon etching, these techniques are important candidates for etching high-resolution holes clear through wafers as Bassous *et al.* [5], [43], [81], [82] first realized and pursued extensively; see Fig. 15. Patterns etched clear through wafers have many potential applications, as will be seen below, but one of the simplest and most commercially attractive is in the area of ink jet printing technology [83], [86]. As shown in Fig. 16(a), the geometry of the pyramidal hole in (100) silicon can be adjusted to completely penetrate the wafer, the square hole on the bottom of the wafer forming the orifice for an ink jet stream. The size of the orifice (typically about 20 μm) depends on the wafer thickness t and mask dimension L according to $l = L - (2t/\tan\theta)$, where $\theta = 54.74^\circ$ is the angle between the (100) and (111) planes. In practice, the dimension l is very difficult to control accurately because 1) wafer thickness t is not easy to control accurately and 2) small angular misalignments of a square mask will result in an effective L which is larger than the mask dimension [43], thereby enlarging l as shown in Fig. 16(b). The angular misalignment error can be eased by using a round mask (*diameter* L) which will give a square hole $L \times L$ independent of orientation, as described in Section III (and Fig. 5(e)) by the general rule of anisotropic undercutting.

Membrane structures have also been used in ink jet nozzle designs not only to eliminate the effects of wafer thickness variations, but also to permit more densely packed orifices as well as orifice shapes other than square. In one technique described by Bassous *et al.* [35], the wafer surface is highly doped with boron everywhere but the desired orifice locations. Next, the wafer is anisotropically etched clear through with EDP as described above, using a mask which produces an l which is 3 to 5 times larger than the actual orifice. Since EDP does not attack silicon which is highly doped with boron, a p^+ silicon membrane will be produced, suspended across the bottom of the pit with an orifice in the center corresponding to the location previously left undoped; see Fig. 16(c). The use of a membrane can also be extended to decrease the minimum allowed orifice spacing. Center-to-center orifice spacing is limited to about 1.5 times the wafer thickness when the simple square geometries of Figs. 15, 16(a)–(c) are employed, but can be much closer using membranes. Orifice spacings in *two* dimensions can be made very small by using (110) oriented wafers and etching vertical-walled *grooves* (as described in Section III) clear through the wafer, aligned to rows of orifices on the other side fabricated by this membrane technique. The result, shown in Fig. 16(d), is a number of closely spaced rows containing arbitrarily spaced holes in a long, narrow rectangular p^+ membrane [35].

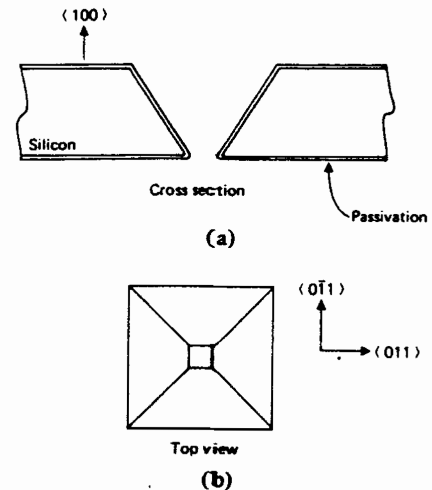


Fig. 15. (a) Cross section and (b) top view of anisotropically etched silicon ink jet nozzle in a (100) wafer developed by E. Bassous *et al.* [5], [43], [8].

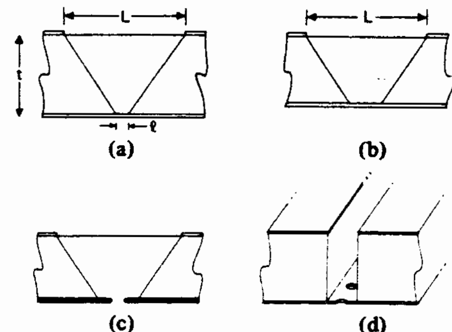


Fig. 16. A number of different methods have been developed for fabricating silicon ink jet nozzles. (a) and (b) show the errors in final nozzle size which occurs when the wafer thickness varies. (c) shows a p^+ membrane structure. This design yields round nozzles and also minimizes the effects of wafer thickness variations. Nozzles can be more closely spaced by using the p^+ membrane technique on a (110) wafer, as shown in (d) [35].

Deep grooves or slots etched clear through (110) silicon have been used by Kuhn *et al.* [87] in another important ink jet application. At a characteristic distance from the ink jet orifice, the ink stream, which is ejected under high pressure, begins to break up into well-defined droplets at rates of about 10^5 drops per second as a result of a small superimposed sinusoidal pressure disturbance. A charge can be induced on individual droplets as they separate from the stream at this point by passing the jet through a charging electrode. Once charged, the drops can be electrostatically deflected (like an electron beam) to strike the paper at the desired locations. Kuhn *et al.* etched

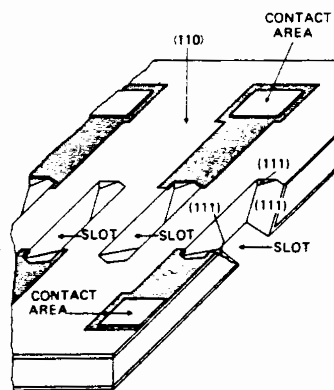


Fig. 17. Grooves anisotropically etched clear through a (110) wafer were employed as charge electrode arrays by Kuhn *et al.* [87] in an ink jet printing demonstration. A charge can be induced on individual ink droplets as they pass through the grooves by applying a voltage to the walls of the groove. Subsequently, drops are "steered" to the paper after traveling through a high electric field. Figure courtesy of L. Kuhn.

several grooves clear through (110) silicon, doped the walls of the grooves so they would be conductive, and defined contact pads connected to the doped sidewalls of the grooves, as shown in Fig. 17. By arranging for the streams to pass through these grooves right at the breakoff points, the grooves can be operated as an array of independent charge electrons. In the design of large, linear arrays of closely spaced ink jet orifices (typical spacing is less than 250 μm), where high precision miniaturized structures are required, silicon micromechanics can provide useful and viable structural alternatives, as long as the usual materials considerations (such as materials compatibility, fatigue, and corrosion) are properly taken into account.

In an effort to integrate ink jet nozzle assemblies more efficiently and completely, another experimental structure was demonstrated in which nozzle, ink cavity, and piezoelectric pressure oscillator were combined using planar processing methods [88]. Orifice channels were first etched into the surface of a (110) oriented wafer as shown in Fig. 18, using an isotropic HNA mixture. After growing another SiO_2 masking layer, anisotropic (EDP) etching was employed to etch the cavity region as well as a deep, vertical-walled groove (which will eventually become the nozzle exit face) clear through the wafer. The wafer must be accurately aligned to properly etch the vertical grooves according to the pattern in Fig. 19. After etching, the silicon appears as seen in Fig. 20(a). The individual chips are separated from the wafer and thick 7740 glass (also containing the supply channel) is anodically bonded to the bottom of the chips. Next, a thin 7740 glass plate (125 μm thick), serving as the pump membrane, is aligned to the edge of the nozzle exit face and anodically bonded to the other side of the silicon chip. The exit orifice, after anodic bonding, is shown in Fig. 20(b). Once the piezo-plate is epoxied to the thin glass plate, a droplet stream can be generated, exiting the orifice at the edge of the chip and parallel to the surface, as shown in Fig. 21.

This planar integrated structure was deliberately specified to conform to the prime requirement of silicon micromechanical applications—no mechanical machining or polishing and minimum handling of individual chips to keep processing and fabrication costs as low as possible. Even though the drops are ejected from the edge of the wafer in this design, the exit face is defined by crystallographic planes through anisotropic etching. Any other nozzle design in which drops are to be ejected parallel to the surface would require an expensive polishing step on the edge of the chip to obtain the necessary smoothness which occurs automatically in this design as a result of inexpensive, planar, batch-processed, anisotropic etching.

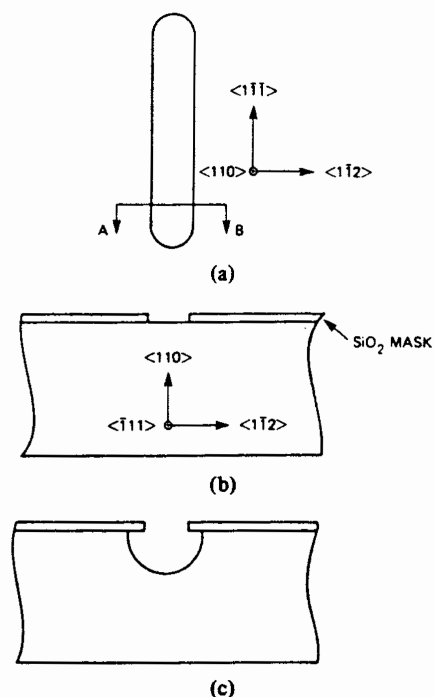


Fig. 18. Orientation and cross section of the isotropically etched nozzle for the planar ink jet assembly after etching. (a) Top view of nozzle channel. (b) Cross section *AB* before silicon etch. (c) After silicon etch. Typical channel depth is 50 μm.

Miniature Circuit Boards and Optical Benches

The packing density of silicon memory and/or circuitry chips can be greatly increased by using silicon essentially as miniature pluggable circuit boards. Two-dimensional patterns of holes have been anisotropically etched clear through two wafers, which are then bonded together such that the holes are aligned as illustrated in Fig. 22. When the resulting cavities are filled with mercury, chips with beam-lead, plated, or electromachined metal probes can be inserted into both sides of the minicircuit board. Such a packaging scheme has been under development for low-temperature Josephson-junction circuits [89]. Dense circuit packaging and nonpermanent die attachment are the primary advantages of this technique. In the case of Josephson-junction circuits, there is an additional advantage in that the entire computer—substrates for the thin-film circuits, circuit boards, and structural supports—are all made from silicon, thereby eliminating thermal mismatch problems during temperature cycling.

Perhaps the most prolific application of silicon anisotropic etching principles is miniature optical benches and integrated optics [90]–[102]. Long silicon V-grooves in (100) wafers are ideal for precise alignment of delicate, small-diameter optical fibers and permanently attaching them to silicon chips. Two cleaved fibers can be butted together this way, for example to accuracies of 1 μm or better. In addition, a fiber can be accurately aligned to some surface feature

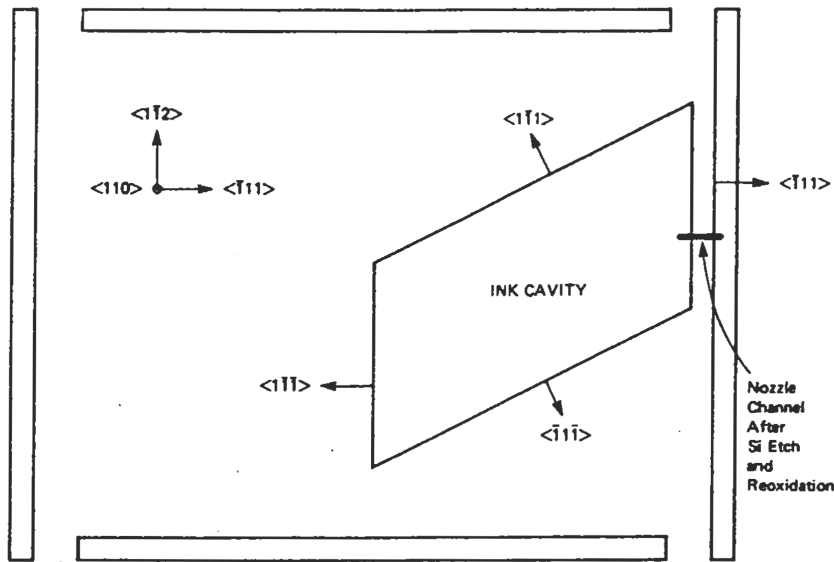


Fig. 19. Orientation of the anisotropically etched ink cavity and deep grooves. After EDP etching, all the (111) surfaces will have flat, vertical walls. Typical cavity size is about 0.5 cm.

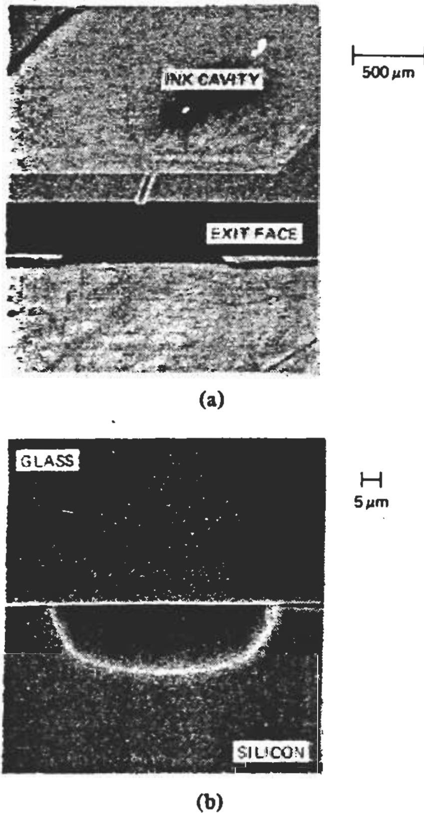


Fig. 20. (a) SEM photograph of silicon nozzle structures after the EDP etch, ready for anodic bonding. Note the nozzle channel which connects the ink cavity to the flat, vertical walls of the exit face. (b) SEM photograph of the ink jet orifice after anodic bonding; glass membrane on top, silicon on bottom.

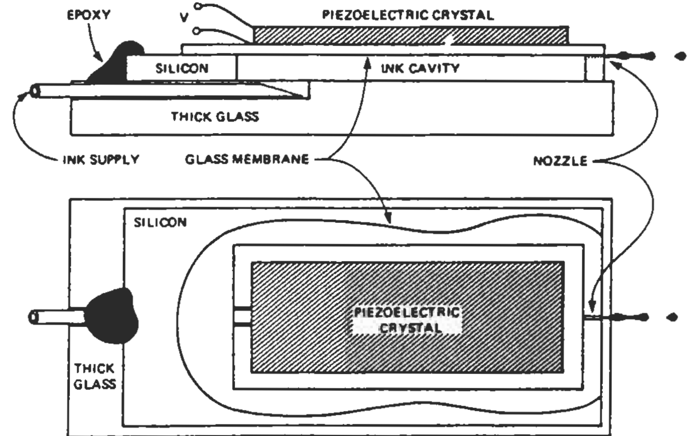


Fig. 21. Schematic of completed nozzle structure showing thick and thin glass plates anodically bonded to either side of the silicon, ink supply line, and piezoelectric ceramic epoxied to the thin glass plate. From [88].

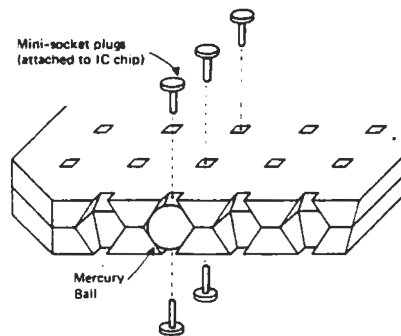


Fig. 22. Complete circuit-board assemblies are under development to optimize the packaging and interconnection of cryogenic Josephson-junction circuits and computers [89]. Miniature socket arrays are created by bonding together two silicon wafers with anisotropically etched holes and filling the cavity with mercury. Miniature plugs attached to the circuit chips themselves are inserted into both sides c the "circuit board." Silicon is used because it can be micromachinec accurately, wiring can be defined lithographically, and thermal mismatch problems are alleviated.

[96], [97], [99], [101], [102]. In Fig. 23(a), a fiber output end is butted up against a photodiode, which can then be integrated with other on-chip circuitry; fiber arrays, of course, are also easily integrated with diode arrays. In Fig. 23(b), a fiber core is accurately aligned to a surface waveguiding layer,

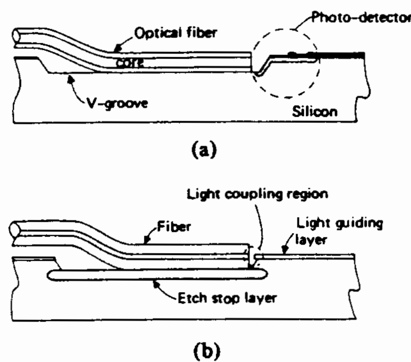


Fig. 23. Silicon is rapidly becoming the material of choice for manipulating fiber-optic components. Two examples are shown here. (a) Coupling a fiber output to a diode detector using an etched V-groove for simple and accurate fiber alignment. (b) Coupling a fiber output to a deposited thin-film optical waveguide using a buried etch-stop layer to obtain precise vertical alignment.

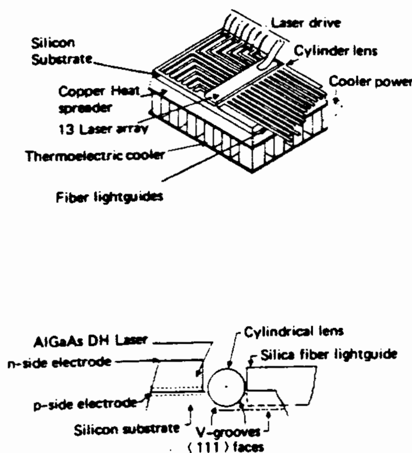


Fig. 24. The most advanced fiber-optic coupling scheme was designed and demonstrated by Crow *et al.* [100]. The output from an array of solid-state lasers was focussed into a corresponding array of optical fibers using another fiber, aligned between the laser array and the output fibers, as a cylindrical condenser lens. All the fibers are aligned by pressing them into accurately aligned V-grooves anisotropically etched into the silicon. Figure courtesy of J. Crow.

by resting the fiber on a buried etch-stop diffusion over which an epitaxial layer has been grown to an accurate thickness.

The most ambitious use of silicon as a mini-optical bench is the GaAs laser-fiber array developed by Crow *et al.* [100]. In this assembly, the light outputs from a perpendicular array of GaAs lasers, mounted on the silicon surface in Fig. 24, are coupled into an optical fiber aligned parallel to the array by one V-groove. This first fiber serves as a cylindrical lens to focus the highly divergent laser light into a perpendicular array of fibers corresponding to the laser array. The linear fiber bundle can now be maneuvered, swept, or positioned independently of the laser package. In addition, this scheme couples the laser light into the fibers very efficiently, while the silicon substrate has the important advantages of serving as an efficient heat sink for the laser array, can be processed to provide isolated electrical contacts and, potentially, on-chip driving electronics to each individual laser in the array.

In addition to fiber alignment aids, such V-grooves, when passivated with SiO_2 and filled with a spun-on polymer, have also been employed as the light-guiding structures themselves [91], [92]. A similar, highly innovative device demonstrated by Hu and Kim also made use of anisotropically etched and

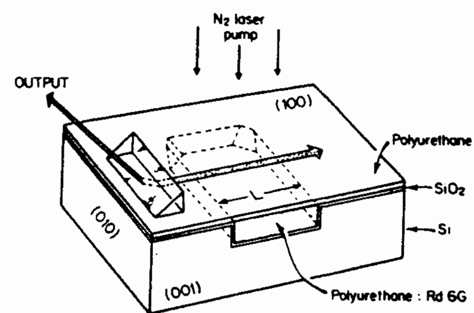


Fig. 25. The high-precision structures of which SCS is inherently capable have included the laser resonator shown here which was demonstrated by Hu and Kim [98]. In this case, sidewalls defined by (100) crystallographic planes have become the perfectly flat and parallel surfaces necessary for the aligned mirrors of a thin-film laser cavity. Figure courtesy of C. Hu.

filled waveguides [98]. When a shallow rectangular well, oriented parallel to the (010) and (001) directions, is etched into a (100) silicon wafer using KOH, the sidewalls of the etched well are defined by these planes and are vertical to the surface. Since the two facing walls of the cavity are ideal, identical crystallographic planes, they are perfectly parallel to each other and normal to the wafer surface. After the wafer is oxidized and spun with a polymer containing a laser dye, the two reflecting, parallel walls of the etched hole (with the dye in between) form a laser cavity. This waveguide laser was optically pumped with a pulsed nitrogen laser by Hu and Kim. Some of the radiation in the cavity itself is coupled out through leakage modes to the thin, excess layer of polymer covering the wafer surface around the laser cavity, as shown in Fig. 25. The output radiation is, of course, in the form of surface guided waves and can be coupled out by conventional integrated optics prism or grating methods.

Gas Chromatograph on a Wafer

One of the more ambitious, practical, and far-reaching applications of silicon micromechanical techniques has been the fully integrated gas chromotography system developed at Stanford by S. Terry, J. H. Jerman, and J. B. Angell [29], [103]. The general layout of the device is illustrated in Fig. 26(a). It consists of a 1.5-m-long capillary column, a gas control valve, and a detector element all fabricated on a 2-in silicon wafer using photolithography and silicon etching procedures. Isotropic etching is employed to generate a spiral groove on the wafer surface 200 μm wide, 40 μm deep, and 1.5 m long. After the wafer is anodically bonded to a glass plate, hermetically sealing the grooves from each other, the resulting 1.5-m-long capillary will be used as the gas separation column. Gas input to the column is controlled by one valve fabricated integrably on the wafer along with the column itself. The valve body is etched into the silicon wafer in three basic steps. First a circular hole is isotropically etched to form the valve cylinder. A second isotropic etch enlarges the valve cylinder while leaving a circular ridge in the bottom of the hole which will serve as the valve seating ring. Finally, holes are anisotropically etched clear through the wafer in a manner similar to ink jet nozzles such that the small orifice exists in the center of the seating ring (see Fig. 26(b)). The flexible valve sealing diaphragm, initially made from a silicon membrane, is now a thin (5–15-μm) nickel button flexed on or off by a small electrical solenoid. Both the valve body and sealing diaphragm are coated with parylene to provide conformal leak-tight sealing surfaces. The sensor, located in the output line of the column,

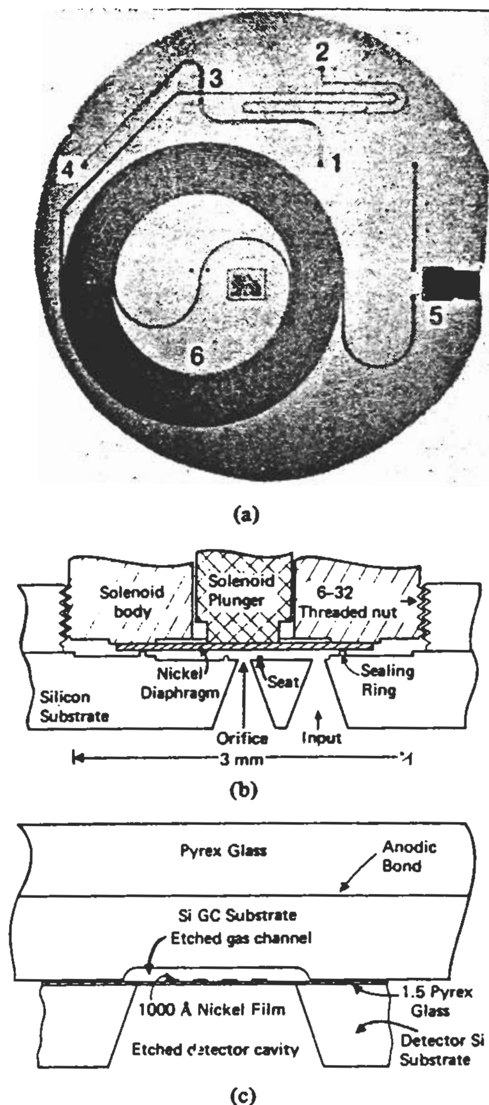


Fig. 26. The most ambitious project utilizing the mechanical properties of silicon is the Stanford gas chromatograph [29], [103]. (a) Overall view of the full silicon wafer showing 1) sample input, 2) purge input, 3) valve region, 4) exhaust of unused sample, 5) sensor region, 6) separation column. The various etched grooves are sealed by anodically bonding a glass plate over the entire wafer. A cross section of the valve assembly is drawn in (b) including the valve cavity, seating ring, and input orifice etched into the silicon as well as the thin nickel diaphragm. The thin-film thermal detector in (c) is also silicon based, consisting of a metal resistor evaporated on SiO_2, thermally isolated by etching the silicon from beneath. Figures courtesy of J. Jerman and S. Terry.

is also based on silicon processing techniques. A thin metal resistor is deposited and etched in a typical meandering configuration over a second oxidized silicon chip. Next, the silicon is anisotropically etched from the back surface of the wafer leaving an SiO_2 membrane supported over the etched hole. This hole is aligned so that the metal resistor is positioned in the center of the membrane and thus thermally isolated from the silicon substrate as shown in Fig. 26(c). The gases separated in the column are allowed to flow over the sensor before being exhausted.

Operation of the column proceeds as follows. After completely purging the system with the inert carrier gas, which flows continuously through port 2 at a pressure of about 30 psi, the valve 3 is opened and the unknown gas sample (held at a pressure higher than the purge gas) is bled into the column through port 1 while the narrow purge supply line appears as a high impedance path to the direction of the sample flow. After introducing a sample with a volume as low as 5 nl, the valve is closed again and purge gas flushes the sample through the column 6. Since the etched capillary is filled with a gas chromatography liner, the various molecular constituents of the sample gas traverse the column at different rates and therefore exit the system sequentially. The sensor element 5 detects the variations in thermal conductivity of the gas stream by biasing the thin, deposited metal resistor at a fixed current level and monitoring its resistance. A burst of high thermal conductivity gas will remove heat from the resistor more efficiently than the low conductivity carrier gas and a small voltage pulse will be detected. A typical signal is shown in Fig. 27. Such a small chromatograph can only operate properly if the sample volume is much smaller than the volur of the column. For this reason, it is essential to fabricate t ultra-miniature valve and detector directly on the wafer with the column to minimize interfering "dead space."

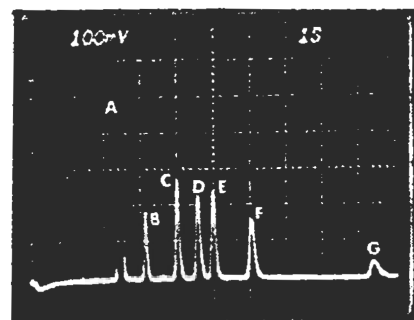


Fig. 27. Example of an output from the miniature gas chromatograph shown in Fig. 26. *A*) nitrogen; *B*) pentane; *C*) dichloromethane; *D*) chloroform; *E*) 111-trichloroethane; *F*) trichloroethylene; *G*) toluene. Photo courtesy of J. Jerman and S. Terry.

A complete, portable gas chromatograph system prototype is being developed by the Stanford group which will continuously monitor the atmosphere, for example, in a manufacturing environment and identify and record 10 different gases with 10 ppm accuracy—all within the size of a pocket calculator.

Miniature Coolers

Besides the Stanford gas chromatograph, the advantageous characteristics of anodic bonding are being employed in even more demanding applications. Recognizing the proliferation of cryogenic sensing devices and circuits based on superconducting Josephson junctions, W. A. Little at Stanford has been developing a Joule-Thomson minirefrigeration system initially based on silicon anisotropic etching and anodic bonding [104]. As shown in Fig. 28, channels etched in silicon comprise the gas manifold, particulate filter, heat exchanger, Joule-Thomson expansion nozzle, and liquid collector. The channels are sealed with an anodically bonded glass plate and a hypodermic gas supply tubing is epoxied to the input and output holes. Such a refrigerator cools down the region near the liquid collector as the high-pressure gas (after passing through the narrow heat exchange lines) suddenly expands into the liquid collector cavity. Little has derived scaling laws for such Joule-Thomson minirefrigeration systems, which show that cooling capacities in the 1-100-mW range at 77 K, cool down rates the order of seconds, and operating times of 100's of hou (with a single gas cylinder) are attainable using a total channel length of about 25 cm, 100 μm in diameter—dimensions simi-

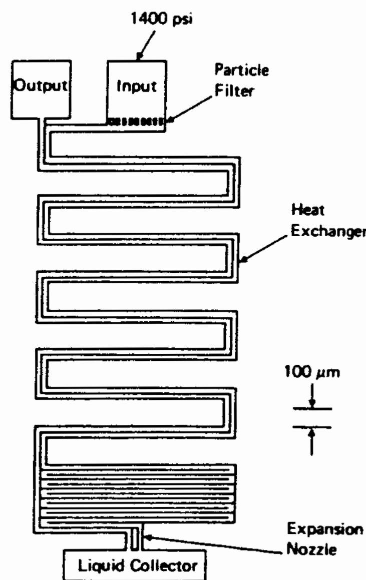


Fig. 28. Grooves etched in silicon have been proposed for the construction of miniature cryogenic refrigerators. In the Joule-Thomson system here, high pressure N_2 gas applied at the inlet expands rapidly in the collection chamber, thereby cooling the expansion region. An anodically bonded glass plate seals the etched, capillary grooves. Adapted from W. A. Little [104].

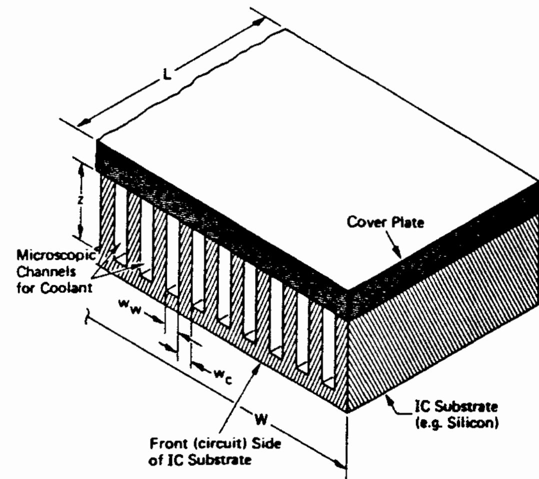


Fig. 29. Schematic view of a compact heat sink incorporated into an integrated circuit chip [105]. For a 1-cm^2 silicon IC chip, using water as the coolant, the optimum dimensions are approximately $w_w = w_c = 57$ μm and $z = 365$ μm. The cover plate is 7740 glass anodically bonded to the silicon, and the channels are anisotropically etched into the (110) wafer with a KOH-based etchant. Thermal resistances less than 0.1 C/W were measured. Figure courtesy of D. Tuckerman.

lar to the gas chromatograph design discussed previously. These lines, however, must not only withstand the thermal shocks of repeated heating and cooling, but also survive the high internal gas pressures (as high as 1000 psi) which occur simultaneously. SCS can be designed to work well in this application cause of its high strength. In addition, the glass/silicon bond ideal not only because of its strength, but also because the nature of the bonding process presupposes an excellent match in thermal coefficients of expansion of the two materials. One disadvantage of silicon in this application is its very high thermal conductivity, even at low temperatures, which limits the attainable temperature gradient from the (ambient) inlet to the liquid collection chamber. Similar all-glass devices have already found use in compact, low-temperature IR sensors and will likely be employed in other scientific instruments from high-sensitivity magnetometers and bolometers to high-accuracy Josephson-junction voltage standards.

As the cycle times of conventional room-temperature computer mainframes and the level of integration of high-speed semiconductor bipolar logic chips continue to increase, the difficulty of extracting heat from the chips in the CPU is rapidly creating a serious packaging problem. Faster cycle times require closer packing densities for the circuit chips in order to minimize signal propagation times which are already significant in today's high-speed processors. This increased packing density is the crux of the heat dissipation problem. Maximum power dissipation capabilities for conventional multichip packaging assemblies have been estimated at 20 W/cm^2. In response to these concerns, a new microcooling technology has been developed at Stanford by Tuckerman and Pease which makes use of silicon micromachining methods [105]. As shown in Fig. 29, a (110) oriented wafer is anisotropically etched to form closely spaced, high aspect ratio oves about $\frac{3}{4}$ of the way through the wafer. A glass plate with fluid supply holes is anodically bonded over the grooves to provide sealed fluid channels through which the coolant is pumped. Input and output manifolds are also etched into the silicon at the same time as the grooves. The circuitry to be cooled is located on the opposite side of the wafer. Over a 1-cm^2 area, a thermal resistance of about 0.1°C/W was measured for a water flow rate of 10 cm^3/s, for a power dissipation capability of 600 W/cm^2 (at a typical temperature rise above ambient of 60°C). This figure is 30 times higher than some previously estimated upper limits.

The use of silicon in this application is not simply an extravagant exercise. Tuckerman and Pease followed a novel optimization procedure to derive all the dimensions of the structure shown in Fig. 29. For optimal cooling efficiency, the fins should be 50 μm wide with equal 50-μm spaces and the height of the fins should be about 300 μm. Fortuitously, these dimensions correspond closely to typical silicon wafer thicknesses and to typical anisotropically etched (110) structures easily realized in practice. Besides the fact that the fabrication of such miniature structures would be extremely difficult in materials other than silicon, severe thermal mismatch problems are likely to be encountered during temperature cycling if a heat-sink material other than silicon were employed here.

The microcooling technique of Tuckerman and Pease is a compact and elegant solution to the problem of heat dissipation in very dense, very-high-speed IC chips. Advantages of optimized cooling efficiency, thermal and mechanical compatibility, simplicity, and ease of fabrication make this an attractive and promising advance in IC packaging. Bipolar chips with 25 000 circuits, each operating at 10 mW per gate (250 W total) are not unreasonable projections for future CPU's, now that a practical cooling method, involving silicon micromechanics, has been demonstrated.

Applications to Electronic Devices

Various isotropic and anisotropic etching procedures have been employed many times in the fabrication of IC's and other silicon electronic devices [106], [107]. In particular, silicon etching for planarization [108], for isolation of high-voltage devices [109], [110], or for removing extraneous regions of a chip to reduce parasitics [111], [112], and in VMOS [113] (more recently UMOS [114]) transistor structures are well-

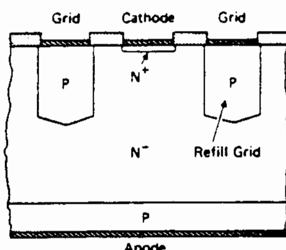


Fig. 30. The deep grid structure of a vertical-channel field-controlled thyristor [58] was accomplished by anisotropically etching deep grooves in the (110) wafer and growing p-doped silicon in the grooves by the epitaxial refill process of Runyan *et al.* and Smeltzer [57] which is shown in Fig. 10(b). Figure courtesy of B. Wessels.

known and some are used extensively in commercial products. Two areas of application in this category deserve special comment in this section, however. The first is a novel technique for producing very deep, doped regions for high-power electronic devices and is based on the epitaxial groove-filling process first demonstrated by Runyon *et al.* and Smeltzer [57] and shown schematically in Fig. 10(b). High-voltage high-power devices require deep diffusions not only to accommodate larger space-charge regions in the silicon (for increased breakdown voltages) but also to carry the larger currents for which such devices are designed. It is not unusual, for example, to schedule high-temperature diffusion cycles lasting over 100 h during some stages in the fabrication of high-power electronic devices. Furthermore, the geometries of such structures are limited because lateral diffusion rates are approximately equal to the vertical rates, i.e., diffusion in silicon is an isotropic process. By anisotropically etching grooves in (110) n-type silicon and refilling them epitaxially with p-type SCS, a process is obtained which appears effectively as an anisotropic diffusion. In this way, very deep, high aspect ratio, closely spaced diffused regions have been realized for high-speed vertical-channel power thyristors such as those demonstrated by Wessels and Baliga [58] (illustrated in Fig. 30), as well as for more complex buried-grid, field-controlled power structures [115]. Similar types of "extended" device geometries have been demonstrated by Anthony and Cline [64] using aluminum thermomigration (see Fig. 11). These micromachining techniques offer another important degree of freedom to the power device designer, which will be increasingly exploited in future generations of advanced high-power devices and IC's.

A second electronic device configuration employing the micromechanical principles discussed here is the V-groove multijunction solar cell [116]. The basic device configuration and a schematic processing schedule are shown in Fig. 31. Fabrication is accomplished by anodically bonding an SiO_2-coated silicon wafer to 7070 glass, anisotropically etching long V-grooves the full length of the wafer completely through the wafer to the glass substrate, ion-implanting p and n dopants into the alternating (111) faces by directing the ion beam at alternate angles to the surface, and finally evaporating aluminum over the entire surface at normal incidence such that the overhanging oxide mask prevents metal continuity at the top of the structure, while adjacent p and n regions at the bottom are connected in series. Solar conversion efficiencies of over 20 percent are expected from this device in concentrated sunlight conditions when the light is incident through the glass substrate. Advantages of these cells are ease of fabrication (one masking step), high voltage (~70 V/cm of cells), long effective light-absorption length (and therefore high

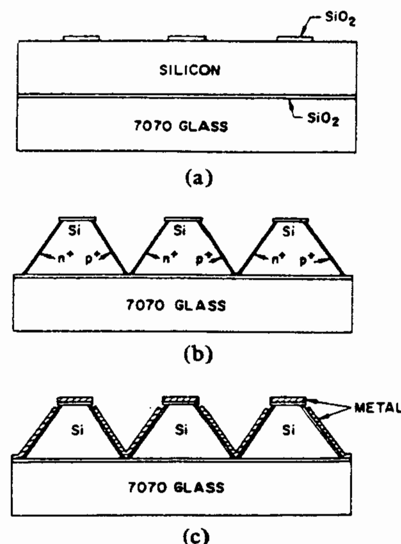


Fig. 31. Major fabrication steps for the V-groove, multijunction solar cell [116]. (a) Grow silicon dioxide layer, field assist bond oxidized wafer to glass, etch pattern windows in silicon dioxide. (b) Anisotropically etch silicon down to 7070 glass substrate, implant n^+ and p^+ regions at an angle, anneal implants. (c) Deposit metallization and alloy. Figure courtesy of T. Chappell.

efficiency) because of multiple internal reflections, no light-blocking metal current collection grid on the illuminated surface, and excellent environmental protection and mounting support provided by the glass substrate. Silicon solar cells based on this technique offer dramatic improvements over present single-crystal designs and may eventually be of commercial value.

V. Silicon Membranes

While the micromechanical devices and components discussed in the preceding section were fabricated exclusively by rather straightforward groove and hole etching procedures, the following applications require some additional processing technologies; in particular, dopant-dependent etching for the realization of thin silicon membranes, which have been discussed in Section III.

X-Ray and Electron-Beam Lithography Masks

An early application of very thin silicon membrane technology which is still very much in the process of development is in the area of high-precision lithography masks. Such masks were first demonstrated by Spears and Smith [117] in their early X-ray lithography work and later extended by Smith *et al.* [118]. Basically, the procedure consists of heavily doping the surface of the silicon with boron, evaporating gold over the front surface, etching the gold with standard photolithographic or electron-beam techniques to define the X-ray mask pattern, and finally etching away most of the silicon substrate from the back side of the wafer (except for some support grids) with EDP [119]. Since heavily boron-doped silicon is not as rapidly attacked by EDP (or KOH), a self-supporting membrane is obtained whose thickness is controlled by the boron diffusion depth, typically 1-5 µm. Since the boron enters the silicon lattice substitutionally and the boron atoms have a smaller radius than the silicon, this highly doped region tends to be under tension as discussed in Section III. When the substrate is etched away, then the member becomes

stretched taut and appears smooth and flat with no wrinkles, cracks, or bowing. X-rays are highly attenuated by the gold layers but not by the thin silicon "substrate" [120], [121]. Several variations on this scheme have been reported. Bohlen *et al.* [122], for example, have taken the X-ray design one step further by plasma etching completely through the remaining thin p^+ silicon regions not covered by gold and using the mask structure for electron-beam proximity printing.

These same basic principles were employed as early as 1966 by Jaccodine and Schlegel [123] to fabricate thin membranes (or windows) of SiO_2 to measure Young's modulus of thermally grown SiO_2. They simply etched a hole from one side of an oxidized Si wafer to the other (using hot Cl_2 gas as the selective etchant), leaving a thin SiO_2 window suspended across the opposite side. By applying a pressure differential across this window, they succeeded in measuring its deflection and determining Young's modulus of the thermally grown SiO_2 layer. Such measurements were later expanded upon by Wilmsen *et al.* [124]. Finally, Sedgwick *et al.* [119] and then Bassous *et al.* [125] fabricated these membrane windows from silicon and Si_3N_4 for use as ultra-thin electron-beam lithography "substrates" (to eliminate photoresist line broadening due to electron backscattering exposures from the substrate) for the purpose of writing very high resolution lines and for use in generating high-transparency X-ray masks. Thin, unsupported silicon nitride windows also have the advantage, in these applications, of being in tension as deposited on the silicon wafer, in the same way that boron-doped silicon membranes are in tension. SiO_2 membranes, such as those studied by Jaccodine and Schlegel [123] and by Wilmsen *et al.* [124], on the other hand, are in compression as deposited, tend to wrinkle, bow, and distort when the silicon is etched away, and are much more likely to break.

Circuits on Membranes

The potential significance of thin SCS membranes for electronic devices has been considered many times. Anisotropic etching, together with wafer thinning, were used by Rosvold *et al.* [111] in 1968 to fabricate beam-lead mounted IC's exhibiting greatly reduced parasitic capacitances. The frequency response of these circuits was increased by a factor of three over conventional diffused isolation methods. Renewed interest in circuits on thinned SCS membranes was generated during the development of dopant-dependent electrochemical etching methods. Theunissen *et al.* [45] showed how to use ECE both for beam-lead, air-gap isolated circuits as well as for dielectrically isolated circuits. Dielectric isolation was provided by depositing a very thick poly-Si layer over the oxidized epi, etching off the SCS substrate electrochemically, then fabricating devices on the remaining epi using the poly-Si as an isolating dielectric substrate. Meek [49], in addition to extending this dielectric isolation technique, realized other unique advantages of such thin SCS membranes, both for use in crystallographic ion channeling studies, as well as large-area diode detector arrays for use in low parasitic video camera tubes.

A backside-illuminated CCD imaging device [126] developed at Texas Instruments depends fundamentally on the ability to generate high-quality, high-strength, thin membranes over large areas. Since their double level aluminum CCD technology effectively blocked out all the light incident on the top surface of the wafer, it was necessary to illuminate the detector array from the backside. In addition, backside illumination improves spatial sensing uniformity and eliminates inference problems associated with front illumination through transparent layers. The high absorption coefficient of silicon in the visible, however, required the imager to be subsequently thinned from the backside (after circuit fabrication) to about 10 µm for efficient collection of photogenerated carriers. It was found that thin, highly uniform membranes could be realized over areas greater than 1 cm^2 with no deleterious effect on the sensitive CCD array and that these membranes exhibited exceptional strength, durability, and resistance to vibration and thermal cycling. Several such large-area CCD imaging arrays (800 × 800 pixels) will be installed in the space telescope scheduled to be launched by the Space Shuttle in 1985.

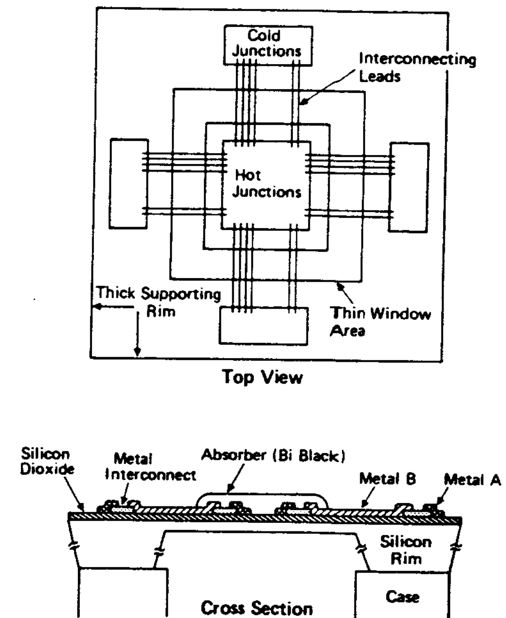


Fig. 32. Thermopile detector fabricated on a silicon membrane [127]. The hot junctions of the Au-poly-Si thermocouples are located in the central region of the membrane, while the cold junctions are located on the thick silicon rim. Efficient thermal isolation, small size, and a large number of integrated junctions result in high sensitivity and high-speed detection of infrared radiation. Figure courtesy of K. D. Wise.

An important aspect of thin insulating membranes is that they provide excellent thermal isolation for thin-film devices deposited on the membrane. Lahiji and Wise [127] have demonstrated a high-sensitivity thermopile detector based on this principle. They fabricated up to 60 thin-film thermocouples (Bi–Sb and Au–polycrystalline Si), wired in series on a 2 mm × 2 mm × 1 µm SiO_2/p^+-Si membrane. Plan and cross-sectional views of this device are shown in Fig. 32. Hot junctions are arranged in the central membrane region while cold junctions are spaced over the thick periphery of the chip. When the membrane is coated with a thin thermal absorbing layer, sensitivities up to 30 V/W and time constants below 10 ms were observed for chopped 500 C black-body radiation incident from the etched (or bottom) surface of the wafer. Such low-mass, thermally isolated structures are likely to be commercially developed for these and related applications.

One thermally isolated silicon structure, in fact, is already commercially available. The voltage level detector of a high-bandwidth ac frequency synthesizer (Models 3336A/B/C) manufactured by Hewlett-Packard [4] is shown in Fig. 33. Two thin silicon cantilever beams with larger masses suspended in the center have been defined by anisotropic etching. The

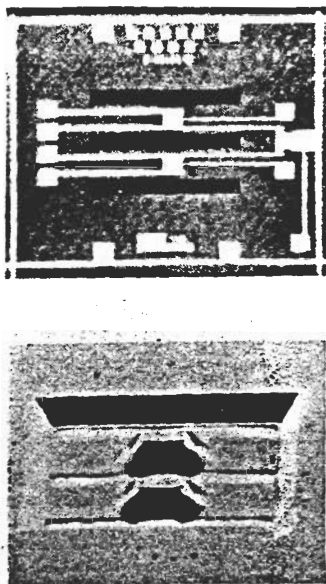


Fig. 33. A high-bandwidth, thermal rms voltage detector [4] fabricated on silicon employs two cantilever beams with matching temperature-sensitive diodes and heat dissipation thin-film resistors on each. This device is used in the output-voltage regulation circuitry of the HP Model 3330 series of frequency synthesizers. Photo courtesy of P. O'Neil.

central masses of each beam are thermally isolated from each other and from the rest of the substrate. Fabricated on each isolated silicon island are a temperature-sensing diode and a thin-film heat-dissipation resistor. When a dc control current is applied to one resistor, the silicon island experiences a temperature rise which is detected by the corresponding diode. Meanwhile, a part of the ac output signal is applied to the resistor on the second island resulting in a similar temperature rise. By comparing the voltages of the two temperature-sensitive diodes and adjusting the ac voltage level until the temperatures of the two diodes match, accurate control of the output ac rms voltage level is obtained over a very large frequency range. This monolithic, silicon thermal converter offers the advantages of batch-fabrication, good resistor and diode parameter matching, while minimizing the effects of ambient thermal gradients. In addition, the masses of the islands are small, the resulting thermal time constants are therefore easy to control, and the single chip is simple to package.

In some applications, great advantages can be derived from electronic conduction normal to SCS membranes. In particular, Huang and van Duzer [128], [129] fabricated Schottky diodes and Josephson junctions by evaporating contacts on either side of ultrathin SCS membranes produced by p^+ doping and anisotropic etching. As thin as 400 Å, the resulting devices were characterized by exceptionally low series resistances, one-half to one-third of that normally expected from epitaxial structures. For Josephson junctions, the additional advantage of highly controllable barrier characteristics, which comes for free with silicon, could be of particular value in microwave detectors and mixers.

Large-area Schottky diodes on SCS membranes with contacts on either side have also found use as dE/dx nuclear particle detectors by Maggiore *et al.* [130]. Since the diodes (membranes) are extremely thin, 1–4 μm, the energy loss of particles traversing the sample is relatively small. This means that heavier ions, which typically have short stopping distances, can be more readily detected without becoming implanted in the silicon detector itself. Consequently, higher sensitivities, less damage, and longer lifetimes are observed in these membrane detectors compared to the more conventional epitaxial detectors.

Thin, large-area, high-strength SCS membranes have a number of other applications related to their flexibility. Guckel *et al.* [131] used KOH and the p^+ etch-stop method to generate up to 5-cm^2 membranes as thin as 2–4 μm. They mounted the structure adjacent to an electroded glass plate and caused it to vibrate electrostatically at the mechanical resonant frequency. Since the membrane is so large (typically 0.8 × 0.8 cm), the resonant frequency is in the audio range 10–12 kHz, yet the Q is maintained at a relatively high value, 23 000 in vacuum, 200 in air.

Pressure Transducers

Certainly the earliest and most commercially successful application of silicon micromechanics is in the area of pressure transducers [132]. In the practical piezoresistive approach, thin-film resistors are diffused into a silicon wafer and the silicon is etched from the backside to form a diaphragm by the methods outlined in Section III. Although the silicon can be etched isotropically or anisotropically from the backside (stopping the etching process after a fixed time), the dimensional control and design flexibility are dramatically improved by diffusing a p^+ etch-stop layer, growing an epitaxial film, and anisotropically etching through the wafer to the p^+ layer. As Clark and Wise showed [133], the membrane thickness is accurately controlled by the epi thickness and its uniformity is much improved. The resistors are located on the diaphragm, near the edges where the strains are largest. A pressure differential across the diaphragm cause deflections which induce strains in the diaphragm thereby modulating the resistor values. Chips containing such membranes can be packaged with a reference pressure (e.g., vacuum) on one side. The first complete silicon pressure transducer catalog, distributed in August 1974 by National Semiconductor, described a broad line of transducers in which the sensor chip itself was bonded to another silicon wafer in a controlled atmosphere, as shown in Fig. 34(a), so that the reference pressure was maintained within the resulting hermetically sealed cavity. This configuration was also described in 1972 by Brooks *et al.* [74] who employed a modified, thin-film anodic bond (as shown in Fig. 13(b)) to seal the two silicon pieces. Silicon eutectic bonding techniques (Au, Au–Sn) and glass-frit sealing are also used frequently in these applications. The National Semiconductor transducer unit is mounted in a hybrid package containing a separate bridge detector, amplifier, and thick-film trimmable resistors. The configuration of Fig. 34(a) suffers from the fact that the pressure to be sensed is incident on the top surface of the silicon chips where the sensitive circuitry is located. Although relatively thick parylene coatings [15] cover the membrane and chip surfaces of this silicon transducer line, it is clear that a different mounting technique is required for many applications in which the unknown pressure can be applied to the less-sensitive backside.

Presently, Foxboro, National Semiconductor, and other companies frequently mount chips in a manner similar to that shown in Fig. 34(b) such that the active chip surface is now the reference side. Chips are bonded both to ceramic and to stainless-steel assemblies. Many commercial sensor units are not yet even hybrid package assemblies and signal conditioning is accomplished by external circuitry. Recently, however, the

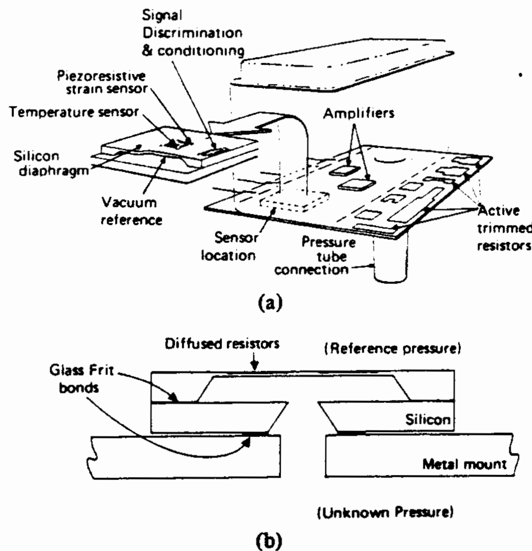


Fig. 34. Piezoresistive pressure transducers have been the earliest and most successful mechanical applications of silicon. At least eight firms now manufacture such sensors, rated for pressures as high as 10 000 psi. (a) Hybrid sensor package marketed by National Semiconductor. The resistor bridge on the silicon diaphragm is monitored by an adjacent detector/amplifier/temperature-compensation chip and trimmable thick-film resistors. Figure courtesy of National Semiconductor Corporation. A cross section of a typical mounted sensor chip is shown in (b). Chip bonding methods include eutectic bonding, anodic bonding, and glass-frit sealing.

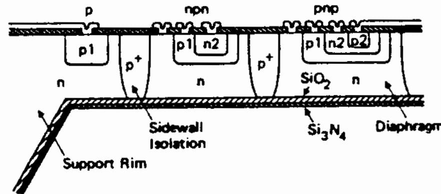


Fig. 35. Piezoresistive silicon pressure transducers with integrated detection and signal conditioning circuitry are now available commercially. Borky and Wise [134] have fabricated a pressure sensor (shown here in cross section) in which the bipolar circuitry is located on the deflectable diaphragm itself. Figure courtesy of K. D. Wise.

Microswitch division of Honeywell has been marketing an integrated pressure transducer chip which incorporates some of the required signal-conditioning circuitry as well as the piezoresistive sensing diaphragm itself. A further indication of future commercial developments along these lines can be seen in the fully integrated and temperature-compensated sensors demonstrated by Borky and Wise [134], and by Ko *et al.* [135]. A cross-sectional view of the membrane transducer fabricated by Borky and Wise, Fig. 35, shows how the signal-conditioning circuitry was incorporated on the membrane itself, thereby minimizing the chip area and providing improved electrical isolation between the bipolar transistors.

Several companies supply transducers covering a wide range of applications; vacuum, differential, absolute, and gauge as high as 10 000 psi. Specific areas of application include fluid flow, flow velocity, barometers, and acoustic sensors (up to about 5 kHz) to be used in medical applications, pneumatic rocess controllers, as well as automotive, marine, and aviation diagnostics. In addition, substantial experience in reliability has been obtained. One of Foxboro's models has been cycled from 0 to 10 000 psi at 40 Hz for over 5×10^9 cycles (4 years) without degradation.

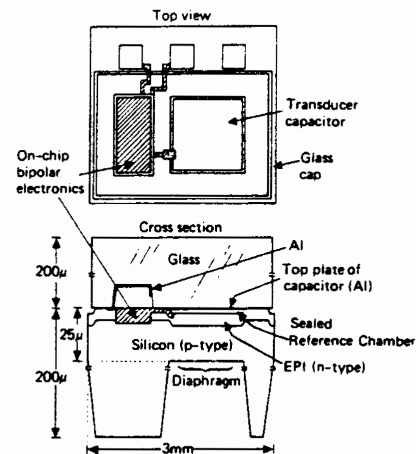


Fig. 36. One silicon diaphragm pressure transducer fully integrated with on-chip electronics is the capacitive sensor assembly demonstrated by Sander *et al.* [136] at Stanford. The design of this device has been directed toward implantable, biomedical applications. An etched glass plate, bonded to the silicon according to Fig. 13(c), hermetically seals the circuitry and also contains the top capacitor electrode. Figure courtesy of J. Knutti.

Few engineering references are available in the open literature concerning the design of silicon pressure transducers. In a recent paper, however, Clark and Wise [133] developed a comprehensive stress-strain analysis of these diaphragm sensors from a finite-element approach. Dimensional tolerances, piezoresistive temperature coefficients, optimum size and placement of resistors, the effects of potential process-induced asymmetries in the structure of the membranes, and, of course, pressure sensitivities have been considered in their treatment.

The sensitivities and temperature coefficients of membrane-based, capacitively coupled (CC) sensors were also calculated by Clark and Wise and found to be substantially superior to the piezoresistive coupled (PC) sensors. For the geometry and mounting scheme, they proposed, however, (with the very thin—2-μm—capacitive electrode gap exposed to the unknown gas), it was concluded that overriding problems would be encountered in packaging and in maintaining the electrode gap free of contaminants and condensates.

Recently, however, a highly sophisticated, fully integrated capacitive pressure sensor has been designed and fabricated at Stanford by C. Sander *et al.* [136]. As shown in Fig. 36, the device employs many of the micromechanical techniques already discussed. A silicon membrane serves as the deflectable element; wells etched into the top 7740 glass plate are used both as the spacer region between the two electrodes of the variable capacitor and as the discharge protection region above the circuitry, the principle of which was discussed in Section III (Fig. 13(c)). Field-assisted thermal bonding seals the silicon chip to the glass plate and assures the hermeticity of the reference chamber (which is normally kept at a vacuum level). The frequency-modulated bipolar detection circuitry is designed to charge the capacitive element with a constant current source, firing a Schmitt trigger when the capacitor reaches a given voltage. Clearly the firing rate of the Schmitt trigger will be determined by the value of the capacitor—or the separation of the capacitor plates. Perhaps one of the more significant aspects of this pressure transducer design is that the fabrication procedure was carefully planned to satisfy the primary objectives and advantages of silicon micromechanics. In particular, the silicon wafer and the large glass plate are

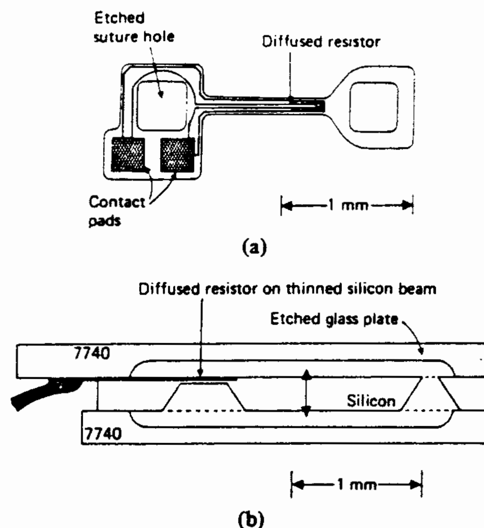


Fig. 37. Research at Stanford has extended the basic piezoresistive pressure sensor concept to complex strain sensor and accelerometer geometries for biomedical implantation applications. The strain sensor (a) contains a diffused piezoresistive element as well as etched suture loops on either end. Figure adapted from [137]. The accelerometer (b) is a hermetically sealed silicon cantilever beam accelerometer [75] sandwiched between two anodically bonded glass plates for passivation and for protection from corrosive body fluids. Figure adapted, courtesy of L. Roylance.

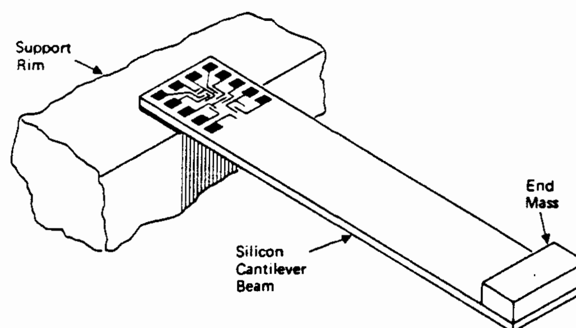


Fig. 38. The mechanical resonant frequency of a silicon cantilever beam was excited in the "Resonistor" by applying a sinusoidal current signal (at 1/2 of the resonant frequency) to a resistor on the silicon surface. These thermal fluctuations cause periodic vibrations of the beam which are detected by on-chip piezoresistive sensors. The signal from the sensor was employed in a feedback loop to detect and stabilize resonant oscillations. The function proposed for the "Resonistor" was a tuned, crystal oscillator. Adapted from Wilfinger *et al.* [138].

both processed using conventional IC techniques, both plates are anodically bonded, and only then is the entire assembly diced up into completed, fully functional transducer chips. Inexpensive batch fabrication methods, as required for practical, commercial silicon IC applications, are followed throughout.

Other Piezoresistive Devices

The principle of piezoresistance has been employed in other devices analogous to pressure transducers. J. B. Angell and co-workers at the Stanford Integrated Circuits Laboratory have advanced this technique to a high level of creativity. His group has been particularly concerned with *in vivo* biomedical applications. Fig. 37(a), for example, shows a silicon strain transducer etched from a wafer which has been successfully implanted and operated in the oviduct of a rabbit for periods exceeding a month [137]. Its dimensions are 1.7 × 0.7 mm by 35 μm thick. Two bonding pads on the left portion of the element make contact to a u-shaped resistor diffused along the narrow central bar. Two suture loops at both ends are also etched in the single-crystal transducer to facilitate attachment to internal tissue. Similar miniature strain transducers, etched from silicon, are now available commercially.

A cantilever beam, microminiature accelerometer, also intended for *in vivo* biomedial studies, is shown in Fig. 37(b). It was developed by Roylance and Angell [75] at Stanford and represents more than an order of magnitude reduction in volume and mass compared to commercially available accelerometers with equivalent sensitivity. Sutured to the heart muscle, it is light enough (<0.02 g) to allow high-accuracy high-sensitivity measurements of heart muscle accelerations with negligible transducer loading effects. It is also small enough (2 × 3 × 0.06 mm) for several to fit inside a pill which, when swallowed, would monitor the magnitude and direction of the pill's movement through the intestinal tract, while telemetry circuitry inside the pill transmits the signals to an external receiver.

Fabrication of the silicon sensor element follows typical micromechanical processing techniques—a resistor is diffused into the surface and the cantilever beam is separated from the surrounding silicon by etching from both sides of the wafer using an anisotropic etchant. The thickness of the thinned region of the beam, in which the resistor is diffused, is controlled by first etching a narrow V-groove on the top surface of the wafer (whose depth is well defined by the width of the pattern as in the case of ink jet nozzles) and, next, a wider V-groove on the bottom of the wafer. When the etched holes on either side meet (determined by continual optical monitoring of the wafer), etching is stopped. The remaining thinned region corresponds approximately to the depth of the V-groove on the top surface. The final form is that of a very thin (15-μm) cantilever beam active sensing element with a silicon (or gold) mass attached to the free end, surrounded by a thick silicon support structure. A second diffused resistor is located on the support structure, but adjacent to the active piezoresistor for use as a static reference value and for temperature compensation. The chip is anodically bonded on both sides to two glass plates with wells etched into them. This sealed cavity protects the active element by hermetically sealing it from the external environment, provides mechanical motion limits to prevent overdeflection, yet allows the beam to deflect freely within those limits. Resonant frequencies of 500 to 2000 Hz have been observed and accelerations of less than $10^{-3}g$ have been detected. Such devices would be extremely interesting in fatigue and yield stress studies.

An early micromechanical device with a unique mode of operation was demonstrated by Wilfinger *et al.* [138], and also made use of the piezoresistive effect in silicon. As shown in Fig. 38, a rectangular silicon chip (typically 0.9 × 0.076 × 0.02 cm) was bonded by one end to a fixed holder, forming a silicon cantilever beam. Near the attached edge of the bond, a circuit was defined which contained a heat-dissipating resistor positioned such that the thermal gradients it generated caused a deflection of the beam due to thermal expansion near the (hotter) resistor, relative to the (cooler) backside of the chip. These deflections were detected by an on-chip piezoresistive bridge circuit, amplified, and fed back to the heating resistors to oscillate the beam at resonance. Since the beam

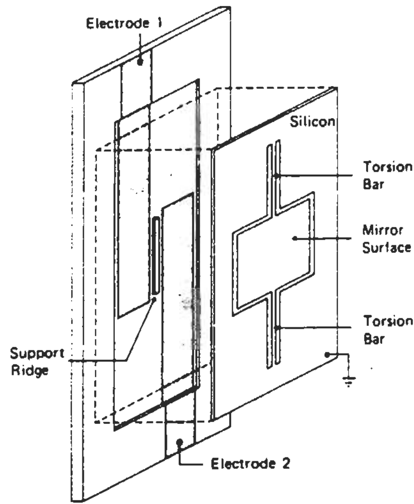


Fig. 39. Exploded view of silicon torsion mirror structures showing the etched well, support ridge, and evaporated electrodes on the glass substrate. From [139].

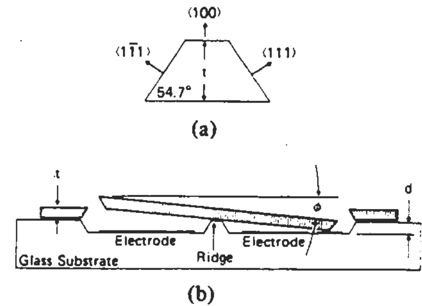


Fig. 40. (a) Cross section of the anisotropically etched torsion bar where t = 134 μm. (b) Cross section of the mirror element defining the deflection angle ϕ, where d = 12.5 μm and a voltage is applied to the electrode on the right.

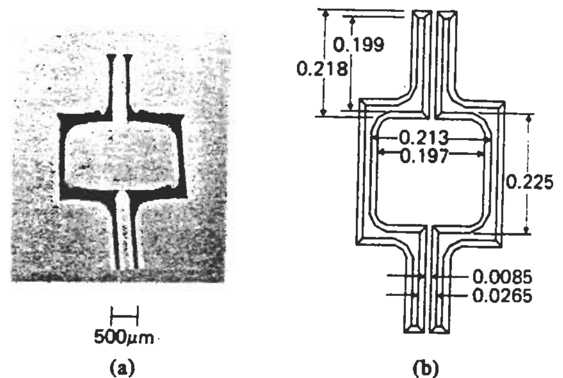


Fig. 41. (a) SEM of typical torsion mirror (tilted 60°) and (b) measured dimensions of 15-kHz mirror element (in cm). The SEM photo is a view of the mirror from the back surface where the electrostatic fields are applied.

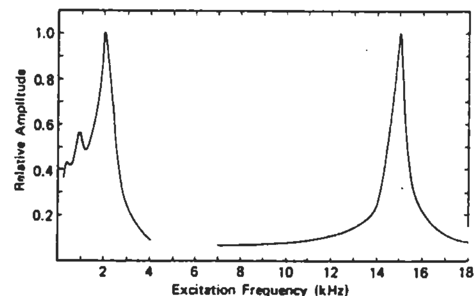


Fig. 42. Deflection amplitude versus drive frequency for two mirrors with differing resonant frequencies.

has a very-well-defined resonant frequency and a high Q (>2000), the output from the bridge exhibits a sharp peak when the heated resistor is excited at that mechanical resonant frequency. This oscillator function has been demonstrated in the range of 1.4 to 200 kHz, and stable, high-Q oscillations were maintained in these beams continuously for over a year with no signs of fatigue.

Silicon Torsional Mirror

This section closes with the description of a device which is not actually a membrane structure, but is related to the strain-measurement mechanisms discussed above and has important implications concerning the future capabilities and potential applications of SCS micromechanical technology. The device is a high-frequency torsional scanning mirror [139] made from SCS using conventional silicon processing methods. An exploded view, shown in Fig. 39, indicates the silicon chip with the anisotropically etched mirror and torsion bar pattern, as well as the glass substrate with etched well, central support ridge, and electrodes deposited in the well. After the two pieces are clamped together, the silicon chip is electrically grounded and a high voltage is applied alternately to the two electrodes which are very closely spaced to the mirror, thereby electrostatically deflecting the mirror from one side to the other resulting in twisting motions about the silicon torsion bars. If the electrode excitation frequency corresponds to the natural mechanical torsional frequency of the mirror/torsion bar assembly, the mirror will resonate back and forth in a torsional mode. The central ridge in the etched well was found to be necessary to eliminate transverse oscillations of the mirror assembly. A cross-sectional view of the torsional bar and of the mirror deflections is shown in Fig. 40. The well-defined angular shapes in the silicon, which are also seen in the SEM (scanning-electron microscope) photograph in Fig. 41(a) (taken from the backside of the silicon chip), result, of course, from the anisotropic etchant. Fig. 41(b) gives typical device dimensions used in the results and the calculations to follow.

Reasonably accurate predictions of the torsional resonant frequency can be obtained from the equation [140]

$$f_R = \frac{1}{2\pi}\sqrt{\frac{12KEt^3}{\rho l b^4(1+\nu)}} \qquad (1)$$

where E is Young's modulus of silicon ($E = 1.9 \times 10^{12}$ dyne/cm^2), t is the thickness of the wafer ($t \sim 132$ μm), ρ is the density of silicon ($\rho = 2.32$ g/cm^3), ν is Poisson's ratio (ν = 0.09) [141], l is the length of the torsion bar, b is the dimension of the square mirror, and K is a constant depending on the cross-sectional shape of the torsion bar ($K \sim 0.24$). For these parameters, we calculate f_R = 16.3 kHz, compared to the experimental value of 15 kHz for the device shown in Fig. 41. The resonant behavior of two experimental torsional mirrors is plotted in Fig. 42.

While complex damping mechanisms, including viscous air-damping and proximity effects due to closely spaced electrodes [142], dominate the deflection amplitudes near resonance, close agreement between theory and experiment can be obtained at frequencies far enough below resonance and at deflection angles small compared to the maximum deflection angle $\phi_{max} = 2d/b$, illustrated in Fig. 43. Under these restric-

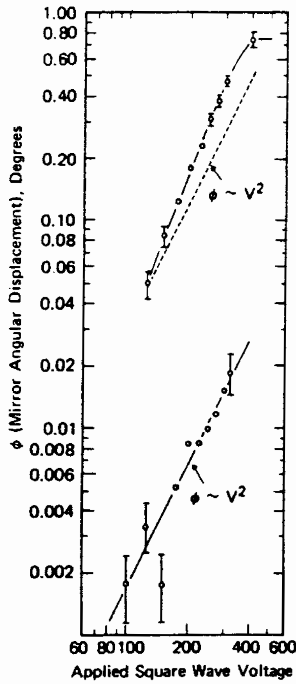


Fig. 43. Experimental deflections of torsion mirror. Resonant displacements are shown at the top, off-resonance at the bottom. Note departure from square-law dependence at resonance.

tions, it can be shown that [143]

$$\phi = \frac{\epsilon_0 V^2 l b^3 (1+\nu)}{16 K E d^2 t^4} A \tag{2}$$

where ϵ_0 is the free-space dielectric permittivity, V is the applied voltage, d is the steady-state electrode/silicon separation, and A is an areal correction factor ($A \sim 0.8$) due to the fact that the active electrode area is somewhat less than half the area of the mirror. We can see from the lower curve in Fig. 43, that the square-law dependence on voltage is confirmed by the data and that the observed deflection amplitudes are only about 20 percent below those predicted by (2). As expected, nonlinearities in the deflection forces are also evident in Fig. 43 during operation at resonance, since the square-law dependence is not maintained.

Optically, silicon possesses an intrinsic advantage over common glass or quartz mirrors in high-frequency scanners because of its high E/ρ ratio, typically 3 times larger than quartz. Using the mirror distortion formulation of Brosens [144], $\frac{1}{3}$ smaller distortions are expected in rapidly vibrated silicon mirrors, compared to quartz mirrors of the same dimensions.

Of prime importance in the study of mechanical reliability is the calculation of maximum stress levels encountered. The maximum stress of a shaft with the trapezoidal cross section of Fig. 38(a) occurs at the midpoint of each side and is given by [145]

$$\tau_{max} \simeq \frac{16KE}{(1+\nu)} \left(\frac{dt}{bl}\right) \tag{3}$$

when the torsion bars are under maximum torque ($\phi = \phi_{max}$). For our geometry, this corresponds to about 2.5×10^9 dyne/cm^2 (36 000 psi), or more than an order of magnitude below the fracture stresses found in the early work of Pearson *et al.* [11]. Reliability, then, is predicted to be high.

This initial prediction of reliability was verified in a series of life tests in which mirrors were continuously vibrated at resonance, for periods of several months. Despite being subjected to peak accelerations of over 3.5×10^6 cm/s^2 (3600 *g*'s), dynamic stresses in the shaft of over 2.5×10^9 dyne/cm^2 (36 000 psi), 30 000 times a second for 70 days ($\sim 10^{11}$ cycles) no stress cracking or deterioration in performance was detected in the SEM for devices which had been properly etched and mounted. After a dislocation revealing etch on this same sample, an enhanced dislocation density appeared near the fixed end of only one of the torsion bars. Since this effect was observed only on one bar, it was presumed to be due to an asymmetry in the manual mounting and gluing procedure, resulting in some unwanted traverse oscillations.

These calculations and observations strongly indicate that silicon mechanical devices, such as the torsion mirror described here, can have very high fatigue strengths and exhibit high reliability. Such results are not unexpected, however, from an analysis of the mechanisms of fatigue. It is well known that, whatever the process, fatigue-induced microcracks initiate primarily at free surfaces where stresses are highest and surface imperfections might cause additional stress concentration points [19]. Since etched silicon surfaces can be extremely flat with low defect and dislocation damage to begin with, SCS structures with etched surfaces are expected, fundamentally, to possess enhanced fatigue strengths. In addition, the few microcracks which do develop at surface dislocations and defects typically grow during those portions of the stress cycle which put the surface of the material in tension. By placing the surface of the structure under constant, uniform compression, then, enhanced fatigue strengths have been observed in many materials. In the case of silicon, we have seen how thin Si_3N_4 films, while themselves being in tension, actually compress the silicon directly underneath. Such layers may be expected to enhance even further the already fundamentally high fatigue strength of SCS in this and other micromechanical applications.

A comparison of the silicon scanner to conventional, commercial electromagnetic and piezoelectric scanners is presented in Table III. The most significant advantages are ease of fabrication, low distortion, and high performance at high frequencies.

VI. Thin Cantilever Beams

Resonant Gate Transistor

Micromechanics as a silicon-based device technology was actually initiated by H. C. Nathanson *et al.* [147], [148] at Westinghouse Research Laboratories in 1965 when he and R. A. Wickstrom introduced the resonant gate transistor (RGT). As shown in Fig. 44, this device consists of a plated-metal cantilever beam, suspended over the channel region of an MOS transistor. Fabrication of the beam is simply accomplished by first depositing and delineating a spacer layer. Next, photoresist is applied and removed in those regions where the beam is to be plated. After plating, the photoresist is stripped and the spacer layer is etched away, leaving the plated beam suspended above the surface by a distance corresponding to the thickness of the spacer film. Typical dimensions employed by Nathanson *et al.* were, for example, beam length 240 μm, beam thickness 4.0 μm, beam-to-substrate separation 10 μm.

Operating as a high-Q electromechanical filter, the cantilever beam of the RGT serves as the gate electrode of a surface MOSFET. A dc voltage applied to the beam biases the transistor at a convenient operating point while the input signal electrostatically attracts the beam through the input force plate,

TABLE III

	Silicon Mirror		Electromagnetic[a]		Piezoelectric[a]	
Fabrication procedure	Batch fabrication of two lithographically processed plates		Complex mechanical assembly of many parts		Two bonded ceramic plates with separate mirror attached	
Frequency scan angle	15 kHz ±1°	50 kHz [b] ±2°	1 kHz ±30°	15 kHz ±2°	1 kHz ±5°	40 kHz ±0.1°
Power	<0.1 W dissipated in drive circuitry		≈0.5 W dissipated in assembly		<0.1 W dissipated in drive circuitry	
Relative distortion	1/3 (silicon mirror)		1 (quartz mirror)		1 (quartz mirror)	
Reliability	≈10^{12} cycles demonstrated		Very high		Very high	
Other	High voltage		High power Heavy assembly		High voltage Off-axis mirror Creep and hysteresis	

a)See Ref. 146.
b)Projected Performance.

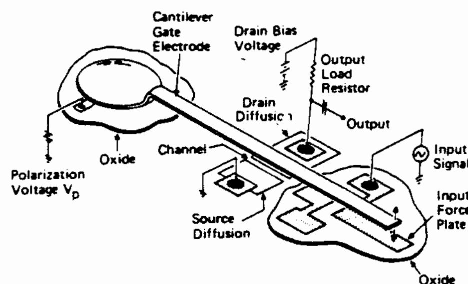


Fig. 44. The earliest micromechanical cantilever beam experiments were conceived at Westinghouse and based on the plated-metal configuration shown here. Operated as an analog filter, the input signal causes the plated beam to vibrate. Only when the signal contains a frequency component corresponding to half the beam mechanical resonant frequency are the beam motions large enough to induce an output from the underlying MOS structure [147], [148]. Figure courtesy of H. Nathanson.

thereby effectively increasing the capacitance between the beam and the channel region of the MOS transistor. This change in capacitance results in a variation of the channel potential and a consequent modulation of the current through the transistor. Devices with resonant frequencies (f_R) from 1 to 132 kHz, Q's as high as 500, and temperature coefficients of f_R as low as 90 ppm°C were described and extensively analyzed by Nathanson *et al.* They constructed high-Q filters, coupled multipole filters, and integrated oscillators based on this fabrication concept. Since the electrostatically induced motions of the beam are only appreciable at the beam resonant frequency, the net Q of the filter assembly is equivalent to the mechanical Q of the cantilever beam. Typical ac deflection amplitudes of the beams at resonance for input signals of about 1 V were ~50 nm.

Practical, commercial utilization of RGT's have never been realized for a number of reasons, some of which relate to technology problems, and some having to do with overall trends in electronics. The most serious technical difficulties discussed by Nathanson *et al.* are 1) reproducibility and predictability of resonant frequencies, 2) temperature stability, and 3) potential limitations on lifetime due to fatigue. The inherent inaccuracies suffered in this type of selective patterned plating limited reproducibility to 20–30 percent over a given wafer in the studies described here. It is not clear if this spread can be improved to much better than 10 percent even with more stringent controls. Temperature stability was related to the temperature coefficient of Young's modulus of the plated beam material, about 240 ppm for gold (the temperature coefficient of f_R is about half this value). Although this problem could be solved, in principle, by plating low-temperature coefficient alloys, such experiments have not yet been demonstrated. Lifetime limitations due to fatigue is a more fundamental problem. Although the strain experienced by the cantilever beam is small ($\sim 10^{-5}$), the stability of a polycrystalline metal film vibrated at a high frequency (e.g., 100 kHz) approaching 10^{14} times (10 years) is uncertain. Indeed, it is known, for example, that polycrystalline piezoelectric resonators will experience creep after continued operation in the 10's of kilohertz. (Single-crystal or totally amorphous materials, on the other hand, exhibit much higher strengths and resistance to fatigue.) These technological difficulties, together with trends in electronics toward digital circuits, higher frequencies of operation (>1 MHz for D/A and A/D conversion), higher accuracies, and lower voltages have conspired to limit the usefulness of devices like the RGT. The crux of the problem is that the RGT filter, while simpler and smaller than equivalent all-electronic circuits, was forced to compete on a basis which challenged well-established conventions in circuit fabrication, which did not take real advantage of its unique mechanical principles, and which pitted it against a very powerful, fast-moving, incredibly versatile all-electronic technology. For all these reasons, conceptually similar devices, which will be discussed below, can only hope to be successful if they 1) provide functions which cannot easily be duplicated by *any* conventional analog or digital circuit, 2) satisfactorily solve the inherent problems of mechanical reliability and reproducibility, and 3) are fabricated by techniques totally compatible with standard IC processing since low-cost high-yield device technologies are most likely only if well-established batch fabrication processes can be employed.

Micromechanical Light Modulator Arrays

The first condition was addressed during the early 1970's when several attempts to fabricate two-dimensional light-modulator arrays were undertaken with various degrees of short-lived success [149]–[152]. Conventional silicon circuits

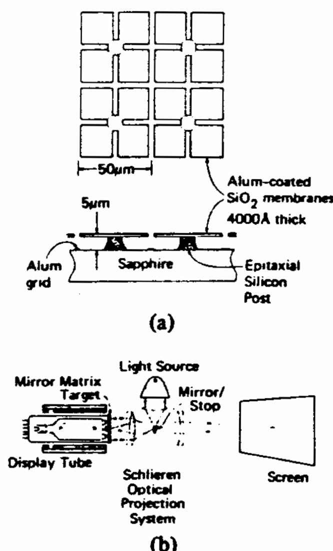


Fig. 45. Taking advantage of the excellent mechanical behavior of thermally grown SiO_2, Westinghouse fabricated large arrays (up to 400 000) of deflectable oxide flaps (0.35 μm thick) and demonstrated an electron-beam addressed image projection display with intrinsic image storage capability [153], [154]. (a) Top view and cross section of oxide flap geometry. The electron-beam addressing and optical projection assembly schematic is shown in (b). Figure courtesy of H. Nathanson.

certainly cannot modulate light. These membrane light modulator arrays were composed of thin (~200-nm) perforated metal sheets, suspended over support structures (~5 μm high) on various substrates. Small segments of the metal sheet behaved as independent mirror elements and could be electrostatically deflected by a scanned electron-beam or by voltages applied to underlying deposited electrodes. The preliminary device demonstrated by van Raalte [149], for example, contained 250 000 individually deflectable thin metal regions. Clearly, the light valve function had not previously been successfully implemented by any other thin-film technology.

Nevertheless, these metal-film designs did not satisfy the second and third requirements. Not only were they potentially susceptible to metal fatigue (gold has a particularly low fatigue strength), but the principles of fabrication were tedious, complex, and intrinsically difficult. In addition, portions of the fabrication process were not even remotely compatible with conventional IC techniques.

During their studies of silicon point field-emitter arrays discussed in Section IV [79], [80], Thomas and Nathanson found that large arrays of deformagraphic elements could also be built using totally conventional and compatible IC processing methods [153], [154]. In addition, while previous workers employed metal films as the deformagraphic material, they used thermally grown amorphous SiO_2 films with fatigue strengths expected to be substantially greater. The structure consisted of a 5-μm silicon epitaxial layer grown over sapphire and covered with a 350-nm-thick thermal oxide. First the oxide is etched into the pattern shown in Fig. 45(a), which defines the final cloverleaf shape of the deflectable oxide membranes. Next, a much thinner oxide is grown and etched away only along the grid lines separating individual light-valve elements. The crucial step involves isotropic etching of the silicon from underneath the oxide elements, undercutting the thin film until only narrow pedestals remain supporting the oxide structures. Finally, the thin oxide remaining in the four slits of each self-supported SiO_2 plate is etched away and the entire array is rinsed and dried. Evaporation of a thin (30-nm) aluminum film makes the oxide beams highly reflective and deposits a metal grid through the openings in the oxide onto the sapphire substrate.

Writing an image on the Mirror-Matrix Display tube is done by raster scanning a modulated electron beam across the target. Each individual mirror element will become charged to a voltage dependent on the integrated incident electron current. Typically, the electron-beam voltage is specified to cause a large secondary electron emission coefficient. The secondaries are collected by a metal grid closely spaced to the target (100 μm) and the mirror metallizations become charged positively. When a negative voltage is then applied to the stationary metal grid on the sapphire surface, electrostatic forces mechanically deflect those elements which have become charged. The pattern of deflected and undeflected beams is illuminated from the backside through the sapphire substrate and the reflected light is projected in a Schlieren optical system such that the deflected beams appear as bright spots on a ground-glass screen. A schematic of the optical and electron-beam illumination systems is shown in Fig. 45(b). Since the metallizations on the mirror surfaces are electrically well insulated from the metal grid on the sapphire surface, charge images can be stored on the deformagraphic array for periods up to many days. At the same time, fast erasure can be accomplished by biasing the external grid negatively and flooding the array with low-energy electrons which equalize the varying potentials across the mirror surfaces.

The particular cloverleaf geometry implemented in the mirror matrix target (MMT) design exhibits very high contrast ratios since the deflected "leaves" scatter light from the optical system at 45° from the primary diffracted radiation. An opaque, cross-shaped stop placed at the focal point of the imaged light beam will only pass that portion of the light reflected from bent "leaves." Contrast ratios over 10:1 have been attained in this way. Over and above the optical advantages, however, the mirror matrix target satisfies all the basic requirements for a potentially practicable micromechanical application. The principles of fabrication are completely compatible with conventional silicon processing; it performs a function (light modulation and image storage) not ordinarily associated with silicon technology; and it greatly alleviates the potential fatigue problems of previous metal-film deformagraphic devices by using amorphous SiO_2 as the active, cantilever beam material. Unfortunately, one of the fabrication problems of the MMT was the isotropic Si etch. Since this step did not have a self-stopping feature, and the dimensions of the post are critical, small etch-rate variations over an array could have a dramatic impact on the yield of a large imaging array.

The MMT has never become a viable, commercial technology primarily because it did not offer a great advantage over conventional video monitors. Image resolution of both video and deformagraphic displays, for example, depend primarily on the number of resolvable spots of the electron-beam system itself (not the form of the target) and, therefore, should be identical for equivalent electron optics and deflection electronics. In addition, since electron-beam scan-to-scan positioning precision is typically not high, it would be very difficult to write on single individual mirrors accurately scan after scan. This means a single written picture element would actually spread, on the average, over at least four mirrors. For an optical image resolution of 10^6 PEL's, then, at least 4×10^6 mirrors would be

required—a formidable task for high-yield photolithography. Finally, the potential savings in the deformagraphic systems due to their intrinsic storage capability is more than offset by the expensive mirror matrix target itself (equivalent in area to at least 20 high-density IC chips when yield criteria are taken into account) as well as the imaging lamp and optics, which are required *in addition to* the electron tube and its associated high-voltage circuits. Historically, high-density displays have always been exceptionally difficult and demanding technologies. While silicon micromechanics may eventually find a practical implementation for displays (especially if silicon-driving circuitry can be integrated on the same chip, matrix addressing the two-dimensional array of mirrors—all electronically), we need not be that ambitious to find important, novel, much-needed device applications amenable to silicon micromechanical techniques.

SiO_2 Cantilever Beams

The full impact of micromechanical cantilever beam techniques was not completely evident until the development of controlled anisotropic undercut etching, as described in Section III. Flexible, fatigue-resistant, amorphous, insulating cantilever beams, co-planar with the silicon surface, closely spaced to a stationary deflection electrode, and fabricated on ordinary silicon with conventional integrated circuitry on the same chip can be extremely versatile electromechanical transducers. A small, linear array of voltage-addressable optical modulators was the first demonstration of this new fabrication technique [155]. Since the method forms the basis of other devices discussed in the rest of this section, we will describe it in some detail. The silicon wafer is heavily doped with boron in those regions where cantilever beams are desired. Since this film will serve as an etch-stop layer during fabrication of the beams, as well as a deflection electrode during operation of the device, the dopant concentration at the surface must be high enough initially to effectively inhibit subsequent anisotropic etching even after the many high-temperature cycles required to complete the structure and its associated electronic circuitry. These additional high-temperature steps tend to decrease the original surface concentration. A level of 7×10^{19} cm^{-3} is usually taken to be the minimum peak value necessary to stop the etchant. Next, an epitaxial layer is grown on the wafer to a thickness corresponding approximately to the desired electrode separation. Since the buried p^+ region is so heavily doped, the electrical quality of the epi grown over these regions may be poor and electronic devices probably should not be located directly above them. At this point, any necessary electronics can be fabricated on the epi-layer adjacent to the buried regions. After depositing (e.g., Si_3N_4) or growing (e.g., SiO_2) the insulating material to be used for the cantilever beam, a thin metal film (typically 30 to 40 nm of gold on chrome) is evaporated and delineated to form the upper electrode. Before silicon etching, care must be taken to insure that the aluminum circuit metallization is adequately passivated since the hot EDP solution will attack these films. Finally, the insulator is patterned as shown in Fig. 46(b), the exposed silicon is etched in EDP to undercut the insulator and free the cantilever beams, and the wafer is carefully rinsed and dried. Since further lithography steps are virtually impossible after the beam is freed, the anisotropic etch is always the last processing step.

As long as the patterns are correctly oriented in (110) directions, undercutting can be completely avoided in unwanted areas as described in Section III. Fig. 47 shows an optical

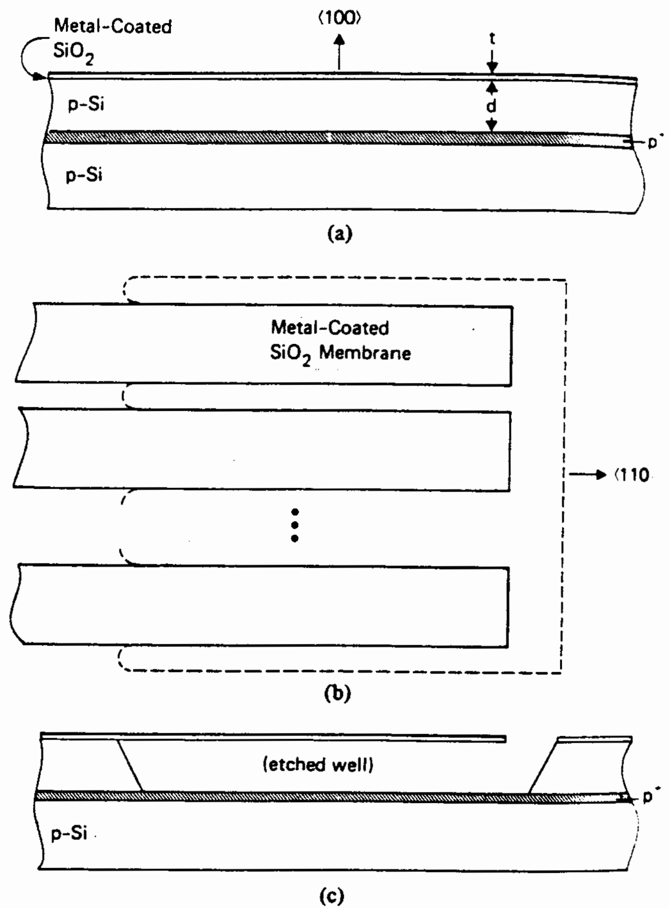
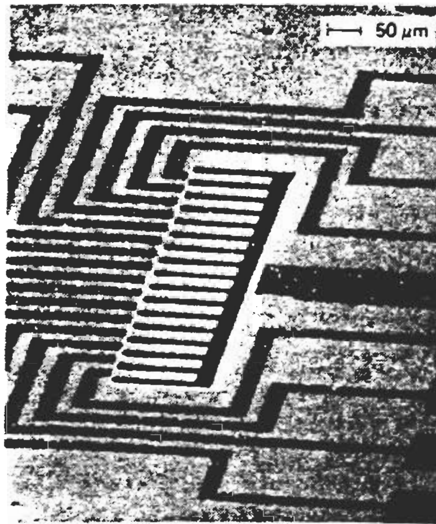


Fig. 46. (a) Cross section of the layers in the linear, cantilever-beam light modulator array. (b) The metal is etched into lines and the oxide is etched from between the lines within the dashed region (top view). (c) The silicon is anisotropically etched from under the oxide to release the beams. From [155]. Each beam can be independently deflected by applying a voltage between the top metallization and the p^+ layer.

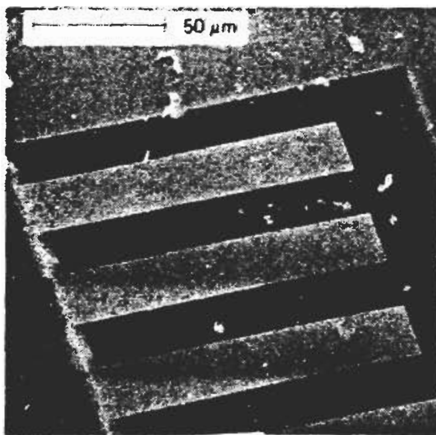
modulator array fabricated in this way. Since the patterns have been oriented correctly, only the beams are undercut, while the periphery of the etched rectangular hole is bounded by the (111) planes. At the same time, the buried p^+ layer stops etching in the vertical direction. The dimensions of the beams in this first demonstration array were 100 μm long made from SiO_2 0.5 μm thick. These are spaced 12 μm from the bottom of the well. A Cr-Au metallization, about 50 nm thick, serves as the top electrode.

Each individual beam can be deflected independently through electrostatic attraction simply by applying a voltage between the top electrode and the buried layer. For low voltages, the deflection amplitude varies approximately as the square of the voltage as indicated in Fig. 48. Both experiment and detailed calculations have shown that once the membrane tip is moved approximately a third of the way down into the etched well, the beam position becomes unstable and it will spontaneously deflect the rest of the way as a result of the rapid buildup of electrostatic forces near the tip. This effect was also analyzed by Nathanson *et al.* [147], [148] for the plated gold RGT beam. In the present geometry, the threshold voltage for spontaneous deflection can be shown to be approximately [156]

$$V_{th} = \sqrt{\frac{3Et^3d^3}{10\epsilon_0 l^4}} \tag{4}$$



(a)



(b)

Fig. 47. SEM photographs of a completed 16-element light modulator array, ready for bonding. Note the high degree of flatness and uniformity of the beams. The SiO_2 beams are 100 μm long, 25 μm wide, and 0.5 μm thick.

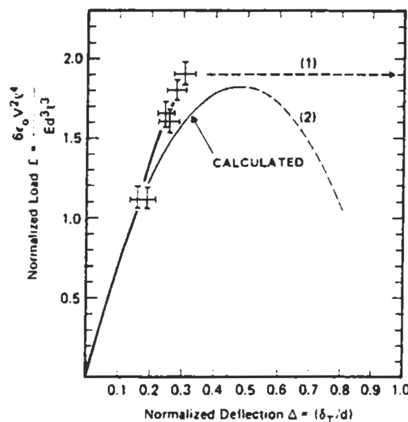


Fig. 48. Calculated beam deflection is plotted here as the lighter line. At the threshold voltage (the peak in the calculated curve), the membrane tip will spontaneously deflect the rest of the way to the bottom of the pit, since its position is unstable along line (2). Experiment data, including the observed spontaneous threshold deflection (along line (1)), are also shown.

where l is the beam length, t is the thickness, ρ is the density, E is Young's modulus, ϵ_0 is the free-space permittivity, and d is the electrode separation. The 16-element array shown in

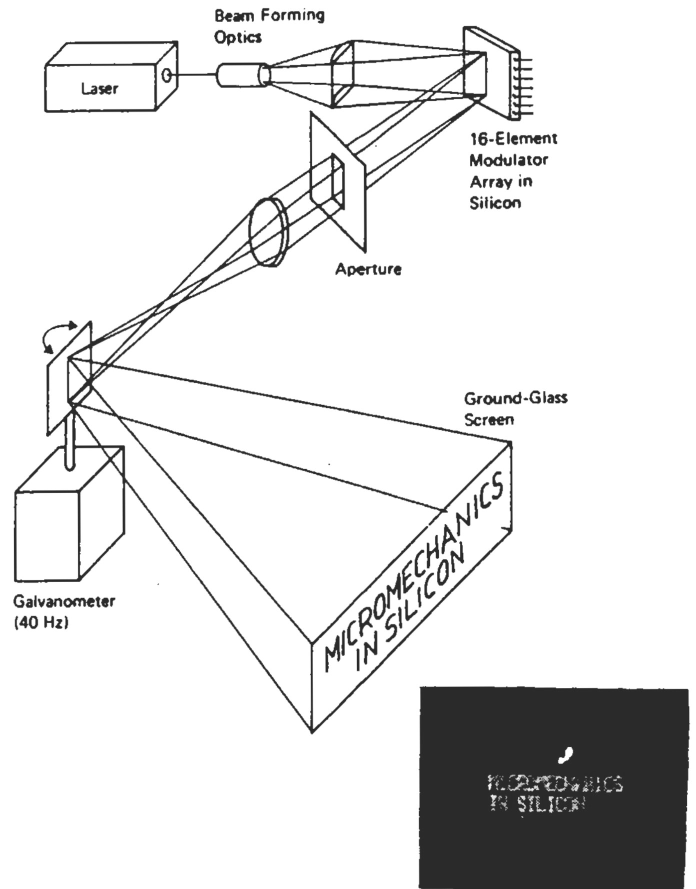


Fig. 49. Schematic of simple optical display employing the 16-beam array in Fig. 47. Each beam is operated as a single modulating element for the corresponding horizontal line in the display. The inset shows a photograph of the display projected onto the ground glass screen.

Fig. 47 was operated below threshold in the simple optical system shown in Fig. 49. A laser was focussed on all 16 mirrors simultaneously while an external aperture was adjusted such that only light reflected from bent membranes was allowed to pass. The resulting vertical line of light, now modulated at 16 points, was then scanned horizontally by a galvanometer to produce a two-dimensional display by rapidly deflecting each membrane independently in the correct sequence. An example of this display is given in the inset in Fig. 49.

Certainly, resonant frequency is an important parameter of such cantilever beams. The first mechanical resonance can be accurately calculated from [157]

$$f_R = 0.162 \frac{t}{l^2} \sqrt{\frac{E}{\rho} K} \tag{5}$$

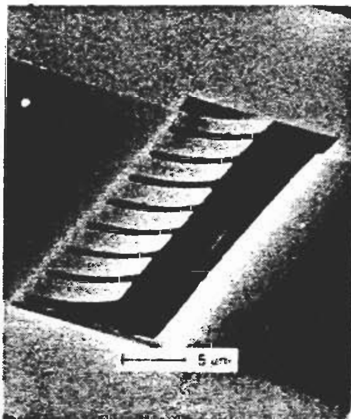
where K is a correction factor (close to one) depending on the density, Young's modulus, and thickness ratios of the metal layer to the insulating layer. For the array given above, f_R = 45 kHz. The highest resonant frequency yet observed is 1.25 MHz for the 8.3-μm-long, 95-nm-thick SiO_2 beams shown in Fig. 50(a).

Once the resonant frequency and the dimensions of a beam are measured, (5) can readily be used to determine Young's modulus of the insulating beam material. Fig. 50(b) shows an array of beams of various lengths fabricated specifically for such measurements. The vibrational amplitude of a reflected optical signal is plotted in Fig. 51 as a function of vibrational frequency for beams of five different lengths. Note that an

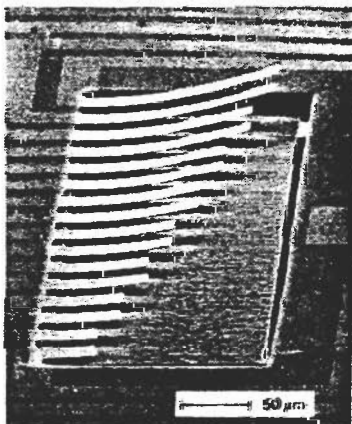
TABLE IV

	Insulator Thickness (Å)	Chromium Thickness (Å)	Assumed Insulator Density (g/cm^3)	Measured Young's Modulus (10^{12} dyn/cm^3)	Published Bulk Young's Modulus (10^{12} dyn/cm^2)
SiO_2 (thermal-wet)	4250	150	2.2	0.57	
SiO_2 (thermal-dry)	3250	150	2.25	0.67	0.7 (fused silica)[a)]
SiO_2 (sputtered)	4000	100	2.2	0.92	
Si_3N_4 (CVD)	3500	100	3.1	1.46	1.5[b)]
Si_3N_4 (sputtered)	2900	100	3.1	1.3	
7059 glass (sputtered)	4200	50	2.25	0.52	0.6 (typ.)[3)]
Nb_2O_5 (sputtered)	8400	50	4.47	0.85	1.6 (Nb_2O_3)[d)]
α-SiC (glow discharge)	8800	50	~3.0	0.85	4.8 (single x-tal)[e)]
Cr (sputtered)	---	---	7.2	1.8	2.8[f)]

[a)]See Refs. 164 and 165.
[b)]See Ref. 164.
[c)]See Ref. 165.
[d)]See Ref. 166.
[e)]See Ref. 10.
[f)]See Ref. 163.



(a)



(b)

Fig. 50. Various beam sizes have been fabricated from various materials for the measurements of Young's modulus. The beams in (a) are 8 μm long and less than 0.1 μm thick—they have a 1.2-MHz mechanical resonant frequency. The array in (b) is made from dry thermal SiO_2 and the beams range in length from 118 to 30 μm.

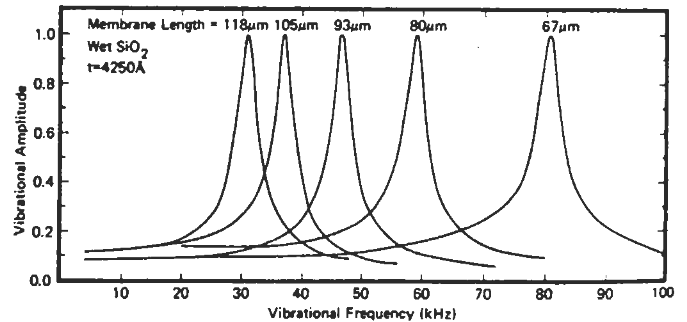


Fig. 51. Resonant behavior measurements of five SiO_2 beams with different lengths to determine Young's modulus of the thermally grown oxide layer.

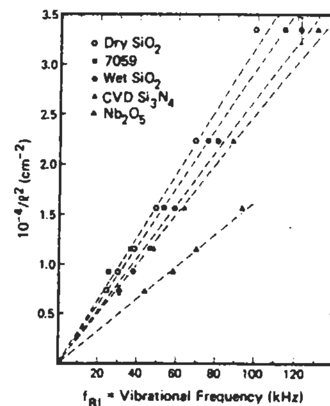


Fig. 52. Determination of Young's modulus according to (5). See Table IV for a complete listing of the films and their parameters. From [158].

electrostatically deflected cantilever beam is a simple frequency doubler because the beam experiences an attractive force for positive as well as negative voltage swings. The resonant frequency is easily detected and can be shown, in Fig. 52, to follow the l^{-2} dependence predicted by (5). A series of measurements on a wide variety of deposited, insulating thin films was undertaken by Petersen and Guarnieri [158], the results of which are tabulated in Table IV. In the past, Young's modulus has been an extremely difficult parameter to measure in thin films due to the fragility of the samples and the concomitant problems in their handling and mounting as well as minutely deforming them and monitoring their motions [159]-[161]. This new, micromechanical technique, on the other hand, is simple, accurate, applicable to a wide range of materials and deposition methods, and useful in many thin-film microstructure studies. Chen and Muller, for example, have fabricated various composite p^+-Si/SiO_2 beams [162], as indicated in Fig. 53, studying their mechanical stability. Such measurements provide additional insight into the nature

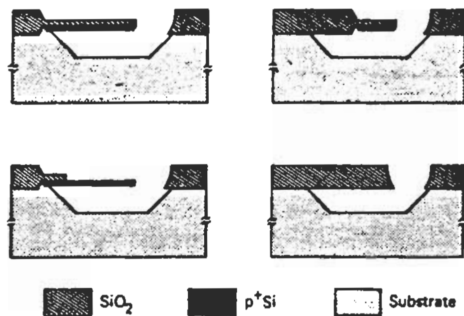


Fig. 53. Miniature cantilever beams of several configurations, including p⁺-Si layers, were fabricated by Jolly and Muller [162] using anisotropic etching together with the p⁺ etch-stop technique, as shown here in cross section. The warpage and stability of the beams were studied as a function of beam length (15–160 μm), width (5–40 μm), and thickness (0.2–0.8 μm). Figure courtesy of R. Muller.

of deposited films, how they differ from the corresponding bulk materials, how they depend on deposition conditions, and how multilayer films interact mechanically.

Integrated Accelerometers

While pressure transducers have been the first commercially important solid-state mechanical transducers, it is likely that accelerometers will become the next. Substantial literature already exists in this area, including the relatively large silicon cantilever beam piezoresistive device of Roylance and Angell which was described in Section V. Closely related to this structure in terms of fabrication principles is the folded cantilever beam accelerometer developed jointly by Signetics Corporation and Diax Corporation [167]. Initial work on the folded beam silicon accelerometer concentrated on piezoresistive strain sensors diffused into the silicon beam, while later studies by Chen *et al.* employed deposited piezoelectric ZnO sensors on identical silicon devices [168]. None of these demonstrations incorporated signal detection or conditioning circuitry on the sensor chip itself, however, as has been accomplished in pressure transducers.

Cantilever beam accelerometers, such as those mentioned above, made by etching clear through a wafer must address serious packaging problems. Special top and bottom motion-limiting plates, for example, must be included in the assembly to prevent beam damage during possible acceleration overshoots. A more problematical issue (which is also a concern in silicon pressure transducers) is the potential for unintentional, residual stresses resulting in hysteresis or drift in the detected signal. Such stresses could be developed, for example, from temperature-coefficient mismatches between the silicon and the various packaging and/or bonding materials.

Small oxide cantilever beams etched directly on the silicon surface alleviate many of the handling, mounting, and packaging problems of solid-state accelerometers since the beam itself is already rigidly attached to a thick silicon substrate. Furthermore, since the active beam element occupies just the top surface of the silicon, potential strains induced during mounting and packaging of the substrate will have little effect on the detector itself. An example of this type of accelerometer is the $ZnO/SiO_2/Si$ composite beam structure demonstrated by Chen *et al.* [169]. As shown in Fig. 54, beam motions induce a voltage across the thin piezoelectric ZnO which is detected and amplified by adjacent, on-chip MOS circuitry. Careful device design and ZnO thin-film deposition techniques have yielded devices with low drift and hysteresis, potential

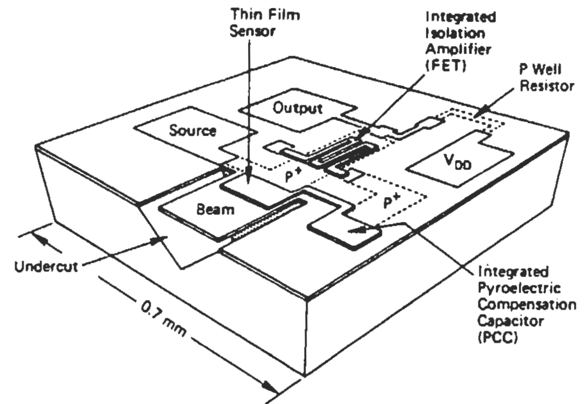
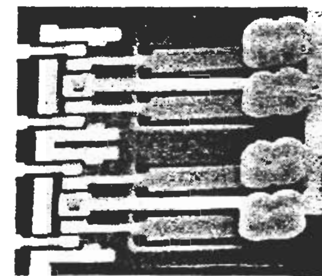
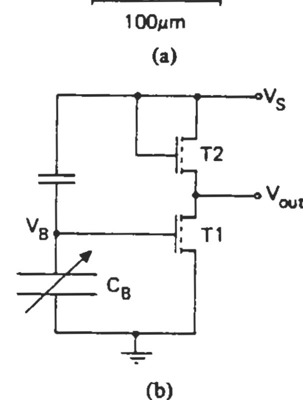


Fig. 54. Layout of the integrated, planar-processed PI-FET accelerometer demonstrated by Chen *et al.* [169]. As the cantilever beam vibrates, voltages induced in the thin-film, ZnO piezoelectric sensor element are detected by the on-chip MOS isolation amplifier. Figure courtesy of R. Muller.



(a)



(b)

Fig. 55. The integrated accelerometer shown here in (a) consists of an SiO_2 cantilever beam sensor (loaded with a gold mass for increased sensitivity) coupled to an MOS detection circuit. The capacitance of the beam (typically 3.5 fF) is employed in a voltage divider network (b) from which small variations in the beam capacitance drive the detection transistor. From [170].

areas of concern when dealing with piezoelectric materials. By completely encapsulating the ZnO layer, for example, charge-storage times on the order of many days were observed. An advantage of the piezoelectric cantilever beam approach is that no buried p⁺ layer is required. One disadvantage is that ZnO is not yet an established commercial technology and may be difficult to adapt to standard IC fabrication procedures.

Another cantilever beam accelerometer [170] also integrated with on-chip circuitry is shown in Fig. 55. As the circuit schematic indicates, the capacitor formed by the p⁺-Si buried layer and the beam metallization are used in a capacitive voltage divider network to bias an MOS transistor in an active operating region, similar to the operating mode of the RGT. Motions

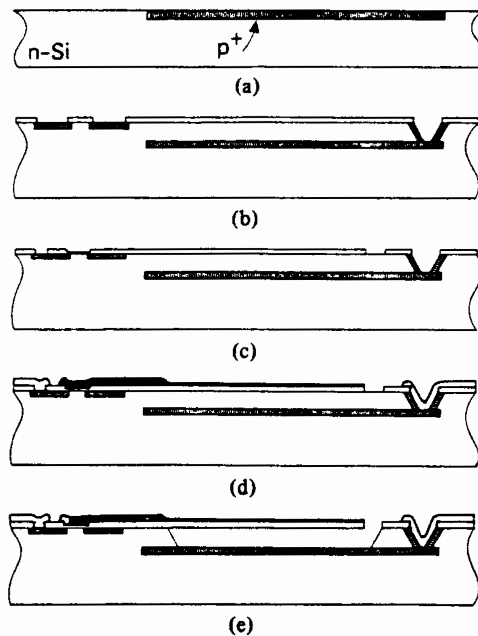


Fig. 56. Abbreviated processing schedule for the integrated accelerometer shown in Fig. 55. (a) Diffusion of p^+ ground electrode and etch stop. (b) Implantation of source, drain, and the sidewalls of the anisotropically etched via. (c) Growth of gate oxide, opening of contact holes, and field oxide etch which defines the geometry of the cantilever beam. (d) Metallization steps including the Al circuit metal, the protective gold overcoat on the Al, and the thin Cr-Au beam metal. (e) Final step in which the silicon is anisotropically etched in a self-stopping procedure to undercut and release the metal-coated SiO_2 cantilever beam.

of the chip normal to the surface can result in movements of the cantilever beam which will modulate the source-drain voltage of the transistor by varying the voltage bias on its gate. Fabrication proceeds according to the schedule shown in Fig. 56. After diffusing the boron-doped buried layer in selected areas and growing n-type epi over the wafer, conventional Al-gate p-channel transistors are defined adjacent to the p^+ regions. Electrical contact to the buried layer is accomplished by doping the sidewalls of a hole anisotropically etched down to the heavily doped region. This diffusion is done at the same time as the source-drain diffusion by a boron-ion-implant step. Next, Al is deposited and etched to form the metal interconnections—even down in the hole used to contact the buried p^+ layer.

Another very thin sputtered Cr-Au layer is deposited and etched for the electrode covering the cantilever beam. This same film is also employed as the plating base to selectively plate a protective Au layer over the already defined aluminum conductors, since the EDP etchant will attack thin Al films. Additional thick gold bumps have also been plated on the ends of the cantilever beams to increase their deflection amplitude with acceleration. Finally, the silicon is anisotropically etched in EDP to free the SiO_2 cantilever beams as described above.

The sensitivity of an SiO_2 beam of thickness t, width b, and length l with a concentrated load at the tip of mass M can be shown to be approximately

$$\Delta V/g = V_s\left(\frac{C_0}{3C_{\text{eff}}}\right)\frac{740 l^4}{Edb^2t^3}M \text{ (V/g of acceleration)} \quad (6)$$

where d is the epi thickness, ϵ_0 is the free-space permittivity, and ρ and E are the density and Young's modulus of SiO_2, respectively. V_s is the circuit supply voltage and C_{eff} is the effective circuit capacitance in the voltage divider network (~120 fF). Also

$$C_0 = \frac{\epsilon_0 lb}{d} \simeq 3.5 \text{ fF} \quad (7)$$

is the equilibrium capacitance between the beam and the buried layer. In good agreement with these calculations, sensitivities of 2.2 mV/g have been measured with loads of 0.35 μg, V_s = −22 V, and beam dimensions of 105 μm by 25 μm and t = 0.5 μm, d = 7 μm. Typical beam motions are about 60 nm/g of acceleration at the beam tip. Capacitance variations as small as 10 aF (corresponding to an acceleration of 0.25g) have been detected with this sensor. Clearly, with such minute equilibrium capacitances, these and other similar miniature solid-state accelerometers *require* on-chip integrated detection circuitry simply to maintain parasitics at a tolerable level. This trend toward higher levels of integration appears to be a continuing feature in many areas of sensor development.

Electromechanical Switches

In 1972, Frobenius *et al.* [171] reported a lithographically fabricated *threshold* accelerometer, conceptually different from the analog devices described above. Based on the plated beam technique developed for the RGT, the tip of the plated beam is allowed to make intermittent contact with another metallization on the surface during large accelerations of the chip normal to its surface. Although this was the first demonstration of a photolithographically generated micromechanical electrical switch, the previously mentioned fatigue problem associated with plated-metal deflectable elements, in addition to its uncertain applicability, halted further development along these lines.

The insulator beam techniques used above for light modulators and accelerators, however, also lend themselves very well to the fabrication of small, fast, integrable, voltage-controlled electrical switching devices which are illustrated schematically in Fig. 57. Such four-terminal switches are not possible with the techniques described by Frobenius because the use of the *insulating* portion of the beam is crucial. Functional micromechanical switching was first realized [156] with a device like that shown schematically in Fig. 57(a). Construction of these switches follows the processing sequence shown in Fig. 58. The first few steps are identical to those employed in the optical modulator array; dope the surface with boron for the vertical etch-stop layer, grow an epitaxial spacer film (about 7 μm), deposit or grow the insulator for the cantilever beam (350-nm SiO_2), deposit a thin Cr-Au metallization (50 nm), delineate the metal lines and the insulator patterns to define the shape of the membrane, which is shown in cross section in Fig. 58(a). Plated metal crossovers and fixed electrode contact points are fabricated in a manner similar to the beams in the RGT and the threshold accelerometer of Frobenius *et al.* First a photoresist layer (PR1) is applied and patterned to provide contact holes through which gold will be plated and to define mesas over which gold will be plated to form the crossover and fixed electrode structures (Fig. 58(b)). Next, a second Cr-Au layer (0.3 μm) is evaporated over the entire wafer to serve as a plating base, and a second photoresist layer (PR2) is applied to define windows through which gold is selectively, electrochemically plated to a thickness of about 2 μm (Fig. 58(c)). After stripping the photoresist layers and excess plating base, the cantilever beams are released by etching the exposed silicon in EDP for about 20 min, then rinsed and dried (Fig. 58(d)).

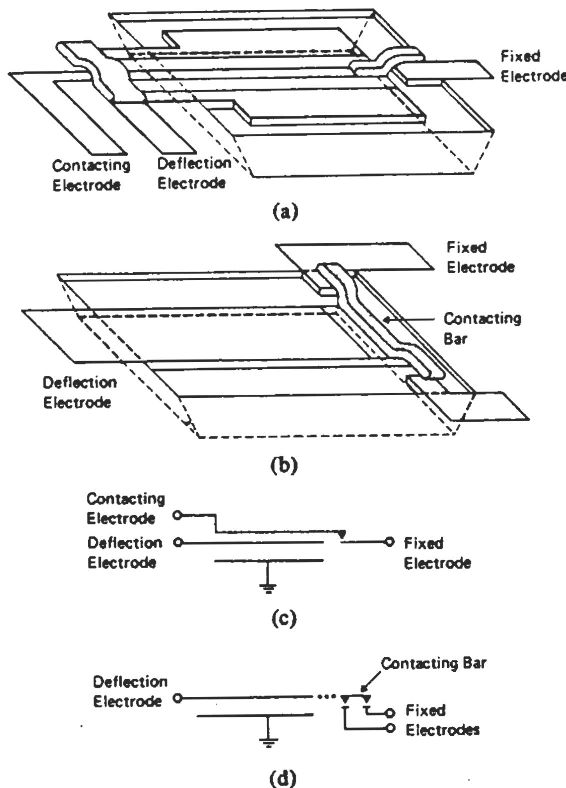


Fig. 57. Two designs of micromechanical switches. (a) The single-contact low-current design. (b) The double-contact configuration. (c) and (d) Suggested circuit representations of these devices. From [156].

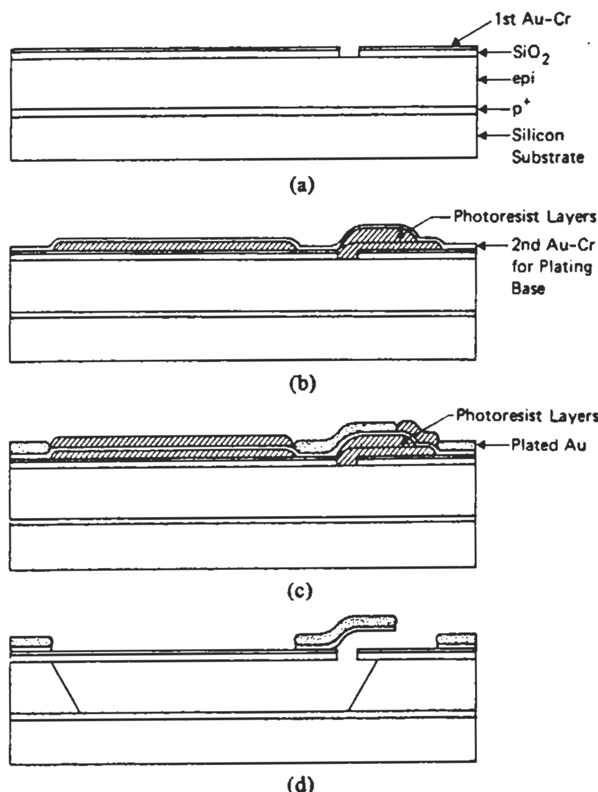


Fig. 58. Cross-sectional diagrams of a single-contact micromechanical switch at various stages during the fabrication procedure. (a) After first metal etch and oxide etch. (b) After evaporation of Au-Cr plating base. (c) After selective Au plating through photoresist holes. (d) Finished structure after photoresist stripping, removal of excess plating base, and EDP etch.

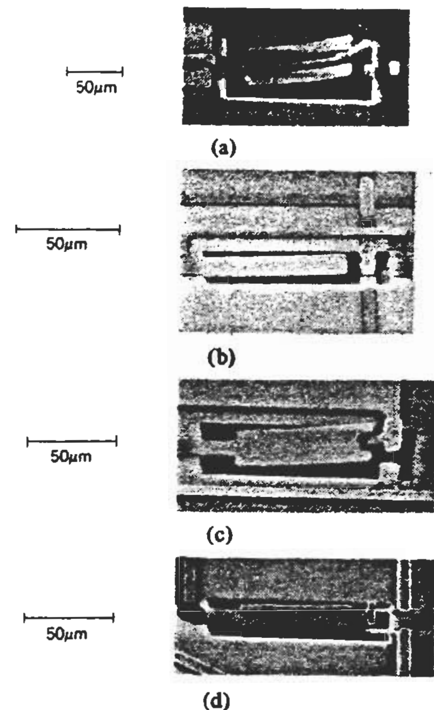


Fig. 59. Four different micromechanical switch designs. (a) Single-contact. (b) Double-contact with a contact bar as shown in Fig. 57(b). (c) and (d) Double-contact designs with two orientations of the fixed electrodes. From [172].

The SEM photographs in Fig. 59 show four different switch configurations, which can be classified as single- or double-contact designs [172]. Electrically, these devices behave as ideal, four-terminal, fully isolated, low-power, voltage-controlled switches. As a voltage is applied between the deflection electrode and the p^+ ground plane, the cantilever beam is deflected and the switch closes, connecting the contact electrode and the fixed electrode. Oscilloscope traces of pulsed switching is shown in Fig. 60. Single-contact switches are simple to operate and were the first to be demonstrated. However, their current-carrying capability is limited to less than 1 mA since all surface metallizations, which extend the length of the cantilever beam (including the current-carrying signal line leading up to the contact bar) must be thin to minimize its influence on the beam's mechanical characteristics. Much higher currents can be switched in the double-contact design since all the signal lines can be plated thick. With one extra masking step, even the fixed electrode regions under the contact bar can be plated prior to the application of the photoresist spacing layers.

While little consideration was given to the details of the contact electrode design in these early switch studies, it is clear that any practical utilization of the devices will rely critically on the ability to maximize current-carrying capability, contact force, reliability, and lifetime by optimizing the metallurgy and the geometry of the contacting electrodes. Gold, for example, is easy to electroplate and is certainly corrosion resistant but may be a poor choice as a contact metal because of its ductility and its self-welding tendency. Equally important is the design and configuration of the contacting surfaces for optimum electrical performance. Clearly, the development of micromechanical switches is in an early stage, yet the versatility of lithography and thin-film processing techniques permit a high degree of engineering design options for such micromechanical structures.

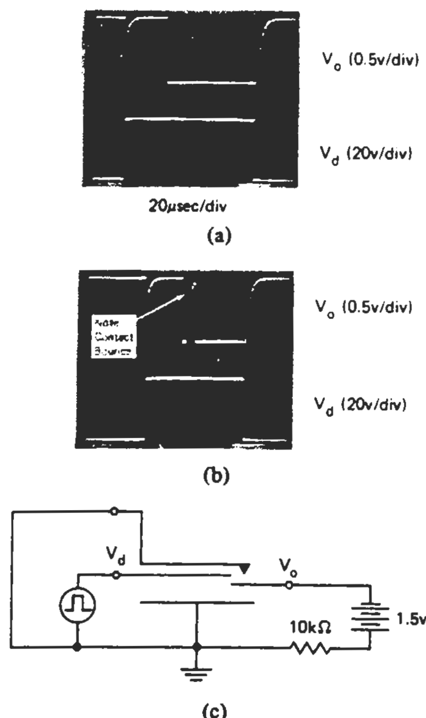


Fig. 60. (a) and (b) Oscilloscope traces of typical pulsed switching behavior for the circuit shown in (c). The deflection voltage in (a) is just above the switching threshold (~60 V), while the voltage in (b) has been increased to about 62 V. Note the delay time (~40 μs) between the application of the deflection voltage and the actual time the switch is closed. For higher deflection voltages (shown in the second oscilloscope trace), delay times are reduced and contact bounce effects are observed.

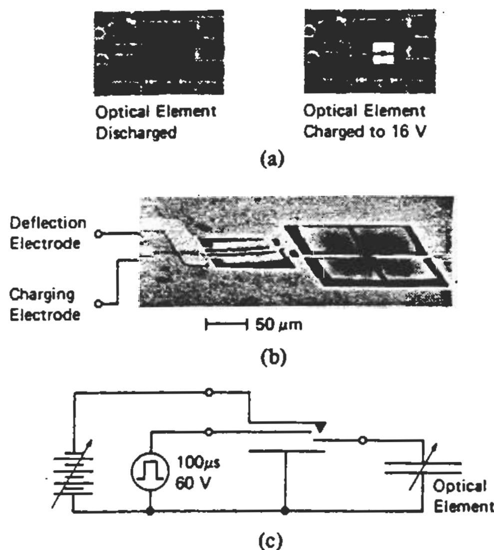


Fig. 61. A charge-storage application of micromechanical switches is illustrated by the circuit of (a) and (b). The capacitor leaves can be charged (and, therefore, deflected) by increasing the charging voltage to 16 V and pulsing the switch on for 100 μs. They will remain stored in this deflected position, shown at the right in (c), until the switch is pulsed again with the charging voltage reduced to zero, thereby releasing the leaves back to their discharged, or undeflected, positions.

Applications of these micromechanical switches range from telephone and analog signal switching arrays, to charge-storage circuits, to temperature [172] and magnetic field sensors. Fig. 61 shows an optical storage cell illustrating the high off-state impedance of which these micromechanical switches are capable. In this device, the charge-storage capacitor is an MMT-type deflectable cloverleaf element. When the switch is activated and the cloverleaf element is charged up to 16 V, the four leaves deflect and appear bright in a dark-field illuminated microscope. Furthermore, cells can be stored for many hours in either the charged (bright) or discharged (dark) condition.

The optimum design of these switches for particular operating parameters involves tradeoffs between the three primary performance criteria of speed, current-carrying capacity, and switching voltage. While the switch resonant frequency (which is related to the switching speed) is given by

$$f_R = \frac{1}{2\pi}\sqrt{\frac{Ebt^3}{4l^3(M + 0.23m)}} \tag{8}$$

where m is the mass of the oxide beam and M is the mass of the plated contact bar, the switching voltage can be expressed approximately as given in (4), repeated here

$$V_{th} = \sqrt{\frac{3Et^3d^3}{10\epsilon_0 l^4}}. \tag{9}$$

From these relationships, we can understand the conflicting requirements for high performance on all aspects of device operation. Since both f_R and V_{th} depend in similar ways on the dimensions of the cantilever beam, high-speed devices imply high switching voltages. While this problem can be alleviated somewhat by reducing the electrode separation d (or epi thickness), the hold-off voltage across the contact electrodes will also be reduced. At the same time, high current capacity implies a large contact metallization M, which also limits switching speed through (8). For the geometries described here, it seems unlikely that resonant frequencies above 200–300 kHz can be realized at voltages less than 20 V in low-current (<1-mA) applications. At the other end of the spectrum, current levels above 1 A might be difficult to obtain in a single device. These micromechanical switch geometries, therefore, are not *very* high speed, nor *very* high current devices, but rather seem to fill a niche between transistors and conventional electromagnetic relays. Other micromechanical switch geometries, however, possibly related to the torsion mirror described in Section V, may be possible which have different ranges of performance.

The advantages of these switches are that they can be batch-fabricated in large arrays, they exhibit extremely high off-state to on-state impedance ratios, the off-state coupling capacitance is very small, switching and sustaining power is extremely low, switching speed is at least an order of magnitude faster than relays, and other electronic devices can easily be integrated on the same chip. Their most serious disadvantages seem to be a relatively high switching voltage (near 50 V) and relatively low current-carrying capability (probably less than 1 A). The ideal applications would be in systems requiring large arrays of medium-current switches or drivers with very low internal resistances. It is still difficult, for example, to integrate large arrays of bipolar drivers with internal resistances less than about 10 Ω.

VII. Silicon Head Technology

An area of particular importance which has already begun to feel the impact of silicon micromechanics is silicon head technology. Heads of all types have common features which are ideally solved by silicon micromechanical techniques. They

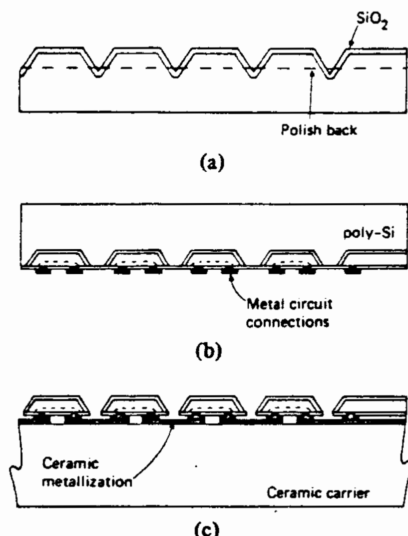


Fig. 62. Fabrication of the thermal print head found in several products manufactured by Texas Instruments is shown here. Based on earlier dielectric isolation schemes, SCS islands are embedded in a polysilicon substrate by a process of etching grooves, depositing SiO_2 followed by the thick poly-Si substrate (250 μm or more), and polishing back the single crystal just until the grooves are penetrated. Next, circuitry is fabricated in the single-crystal islands and the chip is bonded to a ceramic carrier. Finally, the polysilicon is selectively removed. Adapted from Bean and Runyan [175].

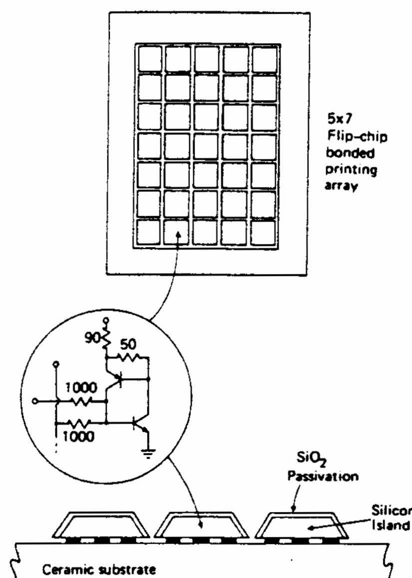


Fig. 63. A 5 X 7 array of silicon islands forms the complete print head in the T.I. Silent 700 computer terminals. Each island is about 25 μm thick and contains the bipolar power latching circuit shown, yet this thin silicon IC chip is also forcefully abraded against the paper while simultaneously thermally cycled to 260°C. Adapted from [174].

typically must be moved rapidly across some surface such as paper, magnetic media, or optical disk and so must be lightweight for high speed, accurate movement, and tracking abilities. In addition, it is always valuable, especially in multichannel heads, to have decoding and driving electronics available as close to the head as possible both to limit flexible wire attachments and to increase signal-to-noise ratios. As printing and recording technologies strive for higher and higher resolution, thin-film methods are being intensely pursued for the design and fabrication of active head elements. Micromechanics offers the potential of using thin-film methods not only for active head elements, but also for the precise micromachining of the passive structural assemblies on which the active head elements are located. Batch-fabrication, materials compatibility, simplified electronic interfaces, increased reliability, and low cost result from this strategy.

Ink jet nozzles have already been extensively discussed in Section IV and it seems probable that some variations on these designs will find their way into products in the 1980's. We will not describe these ink jet applications of silicon head technology further in this section.

Texas Instruments Thermal Print Head

Exploitation of silicon head technology has been successfully implemented in the thermal print head manufactured and sold by Texas Instruments [3]. New generations of high-speed (120 characters per second) print heads are now employed in the TI 780 series computer terminals and the 400 element Tigris plotter/printer [173], [174]. Based on the dielectric isolation process described by Bean and Runyan [175], a very abbreviated schematic of the fabrication procedure is illustrated in Fig. 62. Anisotropic etching is used to etch a grid in a silicon wafer which defines a 5 X 7 array of SCS mesas, for example. After growing an insulating film (SiO_2) over the surface, a thick (10-15-mils) layer of polysilicon is deposited, the wafer is turned upside down, and the single crystal is mechanically polished (or etched) back just until the original mesas are reached as shown in Fig. 62(b). At this stage, typical dimensions of the single-crystal mesas are 250 μm square by 25 μm thick. Conventional bipolar circuit fabrication methods are now used to define circuitry on each individual mesa as well as some peripheral circuitry in the single-crystal region surrounding the mesa array. The circuit metallization is completed by depositing solder or beam-lead connections wherever the circuit makes electrical contact to the ceramic substrate. Finally, the wafer is diced up, each individual die is flip-chip bonded to a ceramic substrate containing thick-film printed metallurgy, and the thick polysilicon layer is completely etched away. The resulting structure is shown in Fig. 63. Each mesa contains a latching circuit, a power transistor, and a power-dissipation resistor. The fabrication technique is designed to thermally isolate the mesas from each other (to inhibit thermal crosstalk) and to provide a controlled rate of heat transport to the ceramic substrate. Under normal operation, the latches on the 35 mesas are all set high or low in a pattern corresponding to the alphanumeric character to be printed, then the thermal dissipation supply voltage is pulsed and the activated mesa circuits are heated to about 260°C for 33 ms, causing dark spots to appear on the thermally sensitive paper in contact with the silicon print head.

In complete contrast to presently accepted practices for handling IC chips, in which the active silicon circuit is carefully sealed up, hidden from view, and diligently protected in sophisticated packages, it is important to realize that this thermal print head design places the silicon in direct, unprotected, and abrasive contact with the paper. Clearly, our traditional views of silicon chips as fragile components, always requiring delicate handling and careful protection, need to be modified. In addition, the micromachining techniques discussed in this review are certainly not limited to the fabrication of thermal print heads and it is likely that other electro-

printing methods will also make use of the principles of silicon head technology.

VIII. Conclusion

While inexpensive microprocessors proliferate into automobiles, appliances, manufacturing equipment, instruments, and office machines, the engineering difficulties and the rapidly increasing expense of interfacing digital electronics with sensors and transducers is demanding more attention and causing lengthy development times. In addition, the general technical trends in instrumentation, communication, and input/output (I/O) devices continue to be in the direction of miniaturization for improved performance [1], [6], [7], [176] and reliability. As we have seen in this review, by employing the low-cost, batch-fabrication techniques available with silicon micromachining methods, many of these sensor and transducer I/O functions can be integrated on silicon, alongside the necessary circuitry, using common processing steps, and resulting in systems with improved performance and more straightforward implementation. Significantly, the interest of the engineering community has risen dramatically in response to these recent trends in I/O technology. Three special issues of the IEEE Transactions on Electron Devices (September 1978 "Three-Dimensional Semiconductor Device Structures," December 1979 "Solid-State Sensors, Actuators, and Interface Electronics," and January 1982 "Solid-State Sensors, Actuators, and Interface Electronics") have been devoted to micromachining and integrated transducer techniques. At least three feature articles have appeared in major trade journals within the past year [177]-[179]. The first issue of a new international journal *Sensors and Actuators* devoted to research and development in the area of solid-state transducers was published in November 1980.

Why are silicon-related I/O applications enjoying such a sudden technical popularity? A large part of the answer comes from the nature of the new, microprocessor-controlled electronics market, in which the costs of the sensors, transducers, and interface electronics exceed the cost of the microprocessor itself [1], [6]. This surprising turn of events was undreamed of 7-8 years ago. Since silicon technology has been so successful in the development of sophisticated, yet inexpensive, VLSI electronic circuits, it seems an obvious extension to employ the same materials and the same fabrication principles to lower the costs of the sensors and transducers as well. The purpose of this review has been to illustrate how this extension might be accomplished for a broad range of applications.

From this applications point of view, it is clear that microprocessors and other computing systems will continue to be employed in every conceivable consumer and commercial product. Since the interface and transducer functions will largely determine the costs of such products, those who have learned to fabricate sensors, transducers, and interfaces in a cost-effective manner will be successful in the areas of computer-controlled equipment, from robots, industrial process controllers, and instruments, to toasters, automobiles, and bathroom scales, to displays, printers, and storage devices.

Given the rapidly accelerating demand for silicon-compatible sensors and transducers, and the corresponding success in demonstrating these various components, it is evident that silicon will be increasingly called upon, not only in its traditional electronic role, but also in a wide range of mechanical capacities where miniaturized, high-precision, high-reliability, and low-cost mechanical components and devices are required in critical applications, performing functions not ordinarily associated with silicon. We are beginning to realize that silicon isn't just for circuits anymore.

Acknowledgment

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