Introduction to Nanotechnology and Nanoscience – Class#4

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Outline

- Top-down Technologies
- Semiconductor & Silicon
- PN junction
- IC Fabrication

- (some materials from Professors Lydia Sohn & Tsu-Jae King Liu)

China's $150 Billion Chip Push Has Hit a Dutch Snag

Europe's largest tech company supplies the machines that can make next-generation semiconductors. But it's isn't selling these to China.

This is where ASML comes in. It's the sole manufacturer of extreme ultraviolet lithography equipment – machines that cost $150 million apiece and can etch microscopic circuit patterns onto semiconductors that are twice as small as the previous generation of technology. That lets customers such as Taiwan Semiconductor Manufacturing Corp. and Samsung Electronics Co. produce ever smaller and more energy-efficient chips.

Extreme Ultraviolet Lithography machines

REUTERS

U.S. bans sales of top Nvidia AI chips to China

Wed, August 31, 2022 at 11:50 PM

STORY: U.S. officials have ordered Nvidia to stop exporting two top computing chips used in artificial intelligence to China.

The order affects its A100 and H100 chips, designed to speed up machine learning tasks… "will address the risk that the covered products may be used in, or diverted to, a 'military end use' or 'military end user' in China."

I-Phone 15

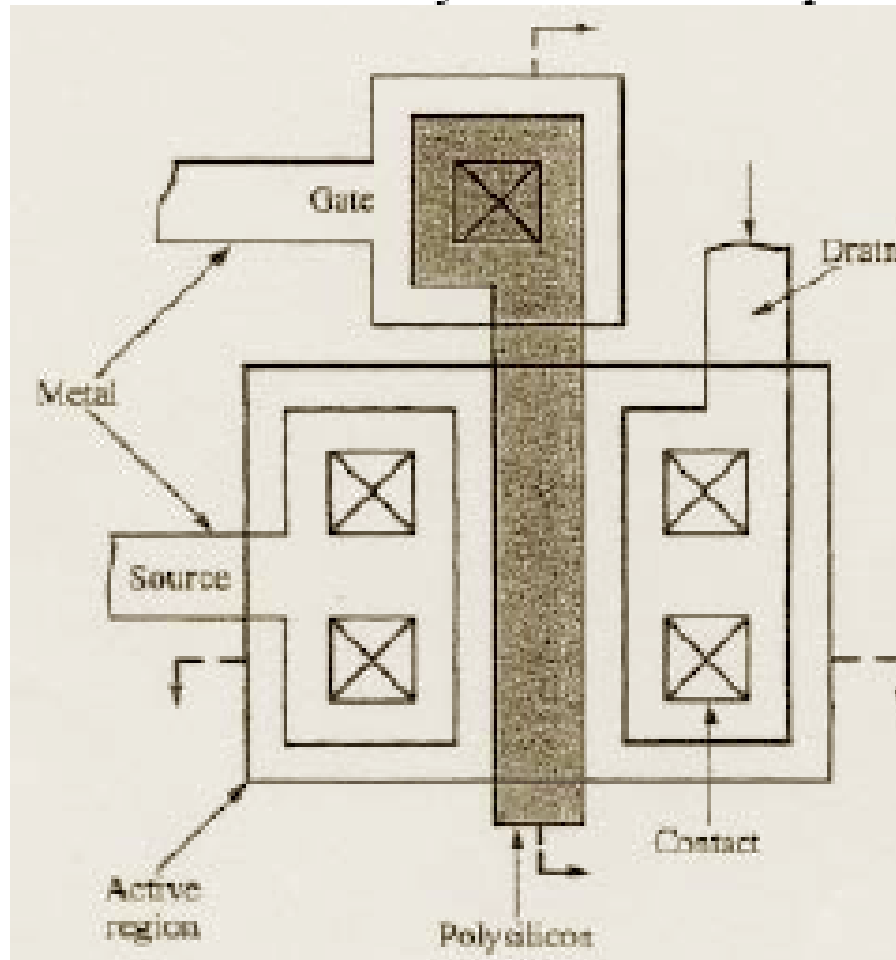
The iPhone 15 Pro is built using a new titanium enclosure. (Apple)

Both the iPhone 15 Pro and iPhone 15 Pro Max also get Apple's new 3-nanometer A17 Pro chips. The chip, which Apple says is the fastest in any smartphone, features 19 billion transistors and features 6 CPU cores broken down into two performance cores and four efficiency cores. There's a 16-core neural engine that Apple says is 2x faster than before.

HW#1 – Problem 4

Problem 4 (MOSFET)

The diagram shows a standard MOSFET. (1) Draw the cross-sectional view diagram in the areas under the two dash lines. (2) Assuming that that the drawing in scale and the minimum feature size is 45nm for the gate length. Calculate how many MOSFET can be placed in an area of 1"x1"



Oxidation in NMOS

Cross-section view

Silicon nitride

SiO_2

p-type silicon

(a)

Top view of masks

Boron implant

p^+

p

(b)

Polysilicon

SiO_2 SiO_2

p^+

p

(c)

Phosphorus or arsenic

SiO_2 SiO_2

n^+ n^+ p^+

p

CVD SiO_2

SiO_2 SiO_2

n^+ n^+ p^+

p

(e)

Al

SiO_2 SiO_2

n^+ n^+ p^+

p

(f)

CMOS

p-substrate
n

(a)

SiO_2
n

(b)

Polysilicon
SiO_2
p
n

(c)

Arsenic implant
Photoresist
n^+
p
n

(d)

Boron implant
Photoresist
n^+
p
n
p^+

(e)

Al
Al
p
n

(f)

Fabrication Methodologies

Millimeter
Micrometer
Nanometer
Angstrom

Top Down

Bulk Material
Thin Film
Heterostructures
Lithographic Wires
Quantum Dots

Z-Axis Gyro
X&Y-Axis Gyro
X,Y,&Z Axis Accelerometer

Nanocrystals
Molecular Wires
Proteins
Molecule
Atom

Bottom Up

- **Microelectronics (CMOS)**
- **Nanostructures (dots, wires, tubes, gap …)**

Top Down: Photolithography

1 PHOTORESIST

SiO_2 LAYER

Si_3N_4 LAYER

Si SUBSTRATE

PREPARED Si WAFER

PROJECTED LIGHT

RETICLE (OR MASK)

2 LENS

PATTERNS ARE PROJECTED REPEATEDLY ONTO WAFER

3 EXPOSED PHOTORESIST IS REMOVED

4 AREAS UNPROTECTED BY PHOTORESIST ARE ETCHED BY GASES

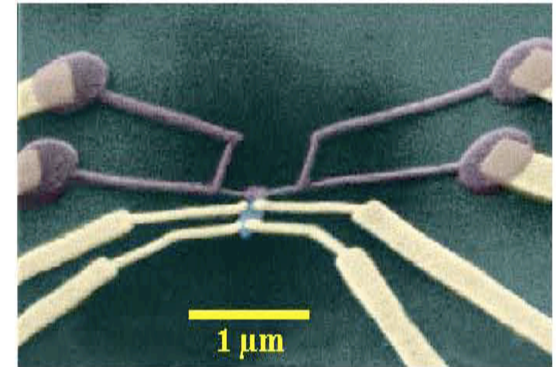
5 IONS SHOWER THE ETCHED AREAS, DOPING THEM

DOPED REGION

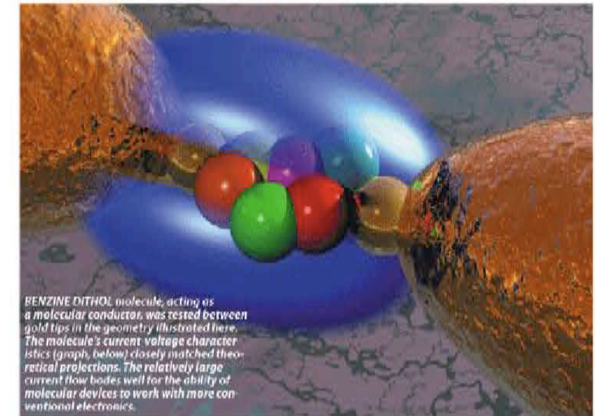
NEW PHOTORESIST IS SPUN ON WAFER AND STEPS 2 TO 4 ARE REPEATED

6 SIMILAR CYCLE IS REPEATED TO LAY DOWN METAL LINKS BETWEEN TRANSISTORS

METAL CONNECTOR

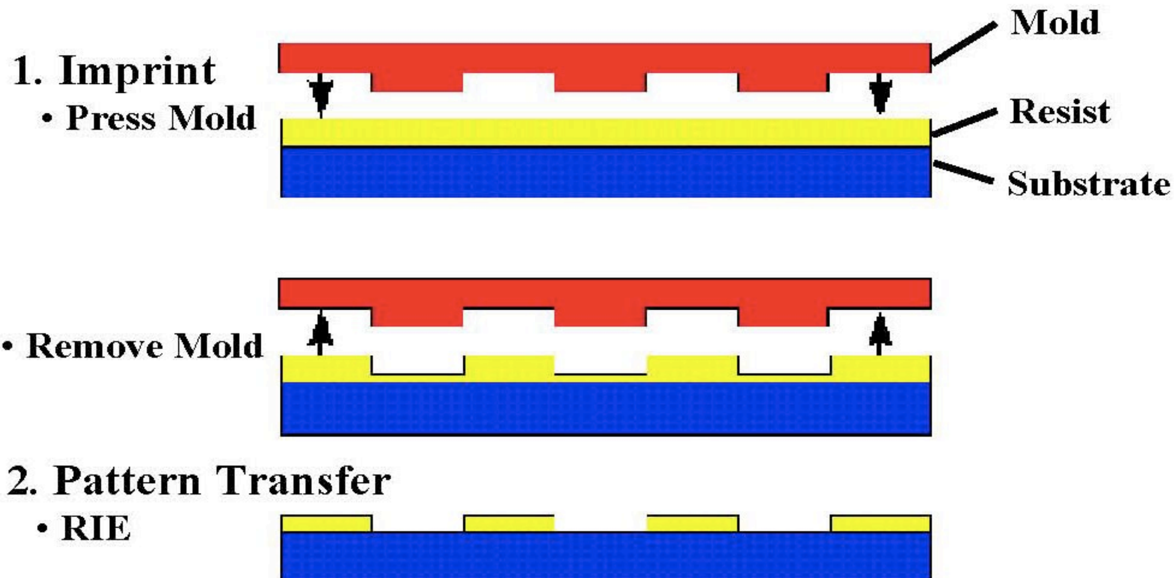


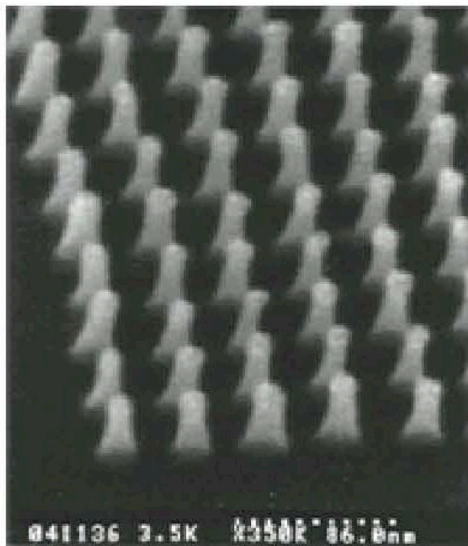
Ferromagnetic/superconducting devices (e-beam lithography)

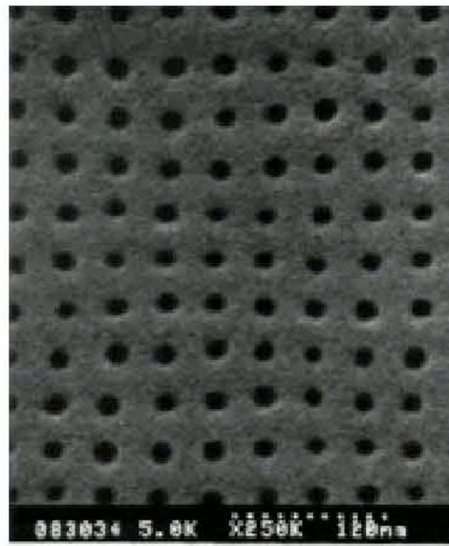


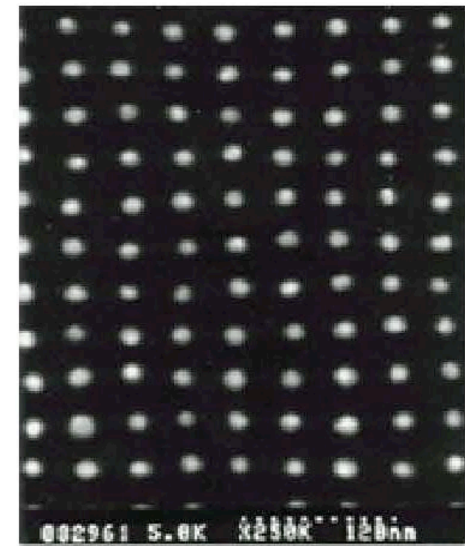
Molecular electronics (e-beam lithography)

Top Down: NanoImprinting



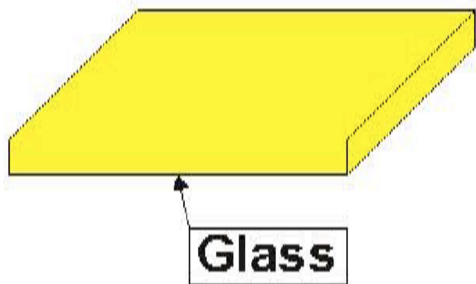




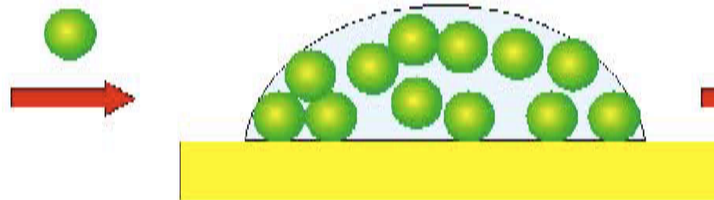


Top Down: Nanosphere Lithography

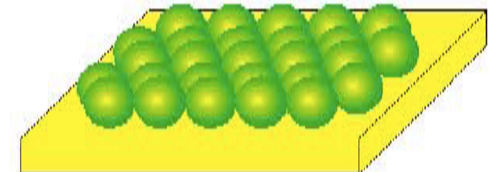
1. Clean Substrate

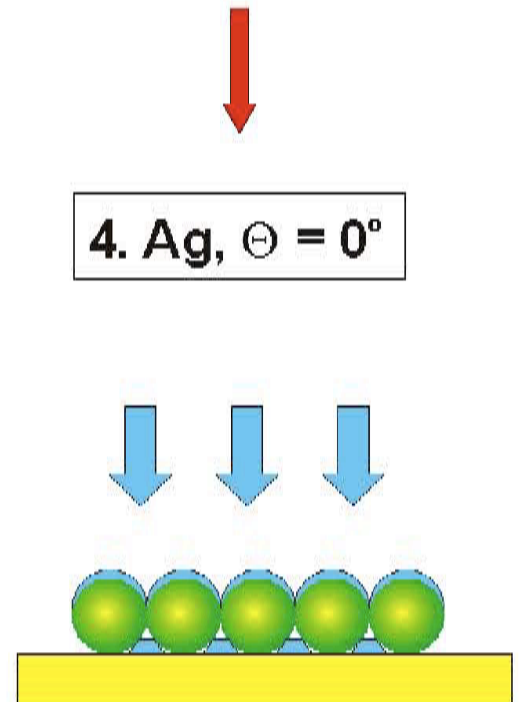


2. Drop Coat

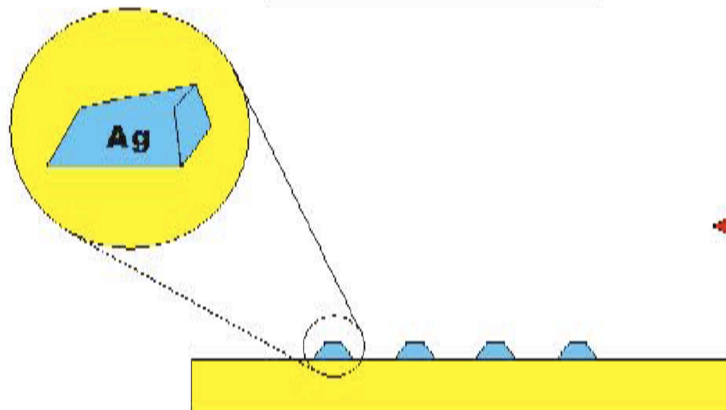


3. Dry

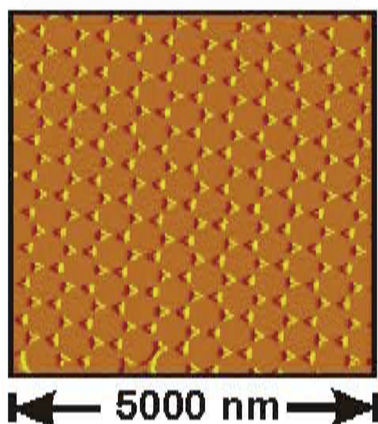




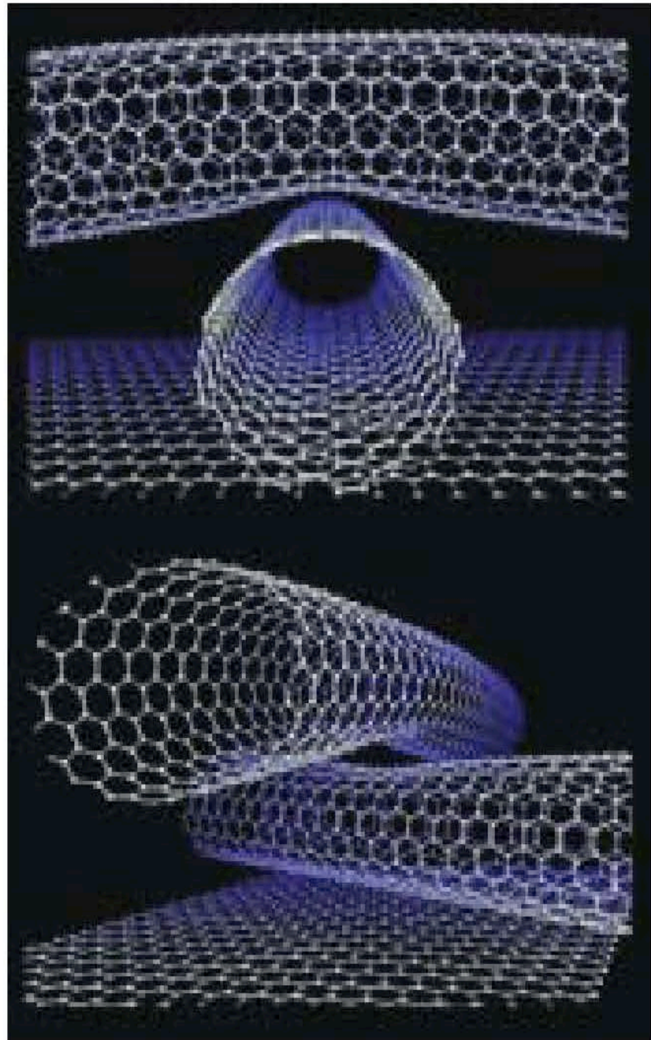
5. Liftoff

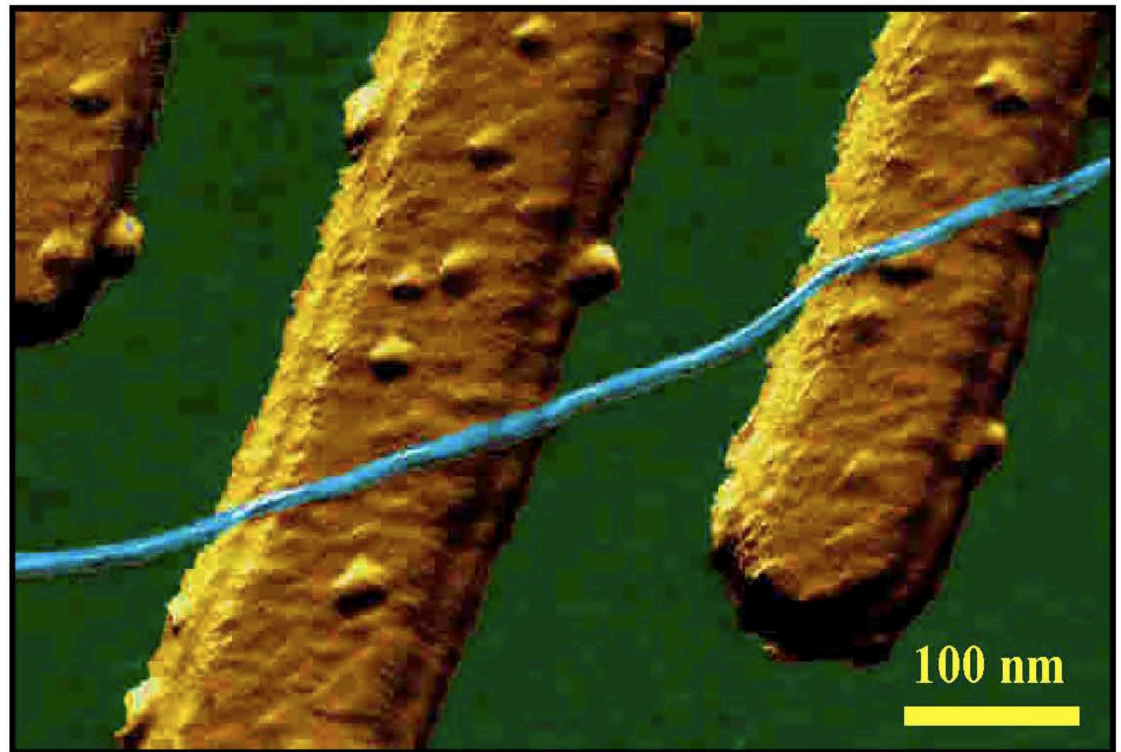


6. AFM



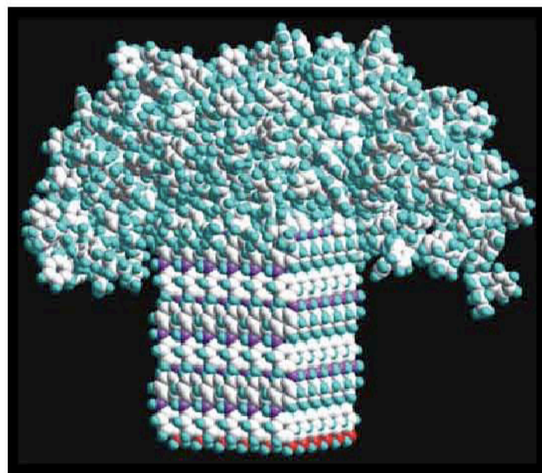
Bottom Up: Carbon Nanotube Synthesis



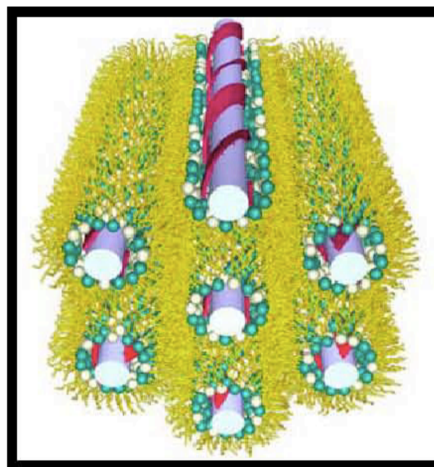


Bottom Up: Molecular Self Assembly

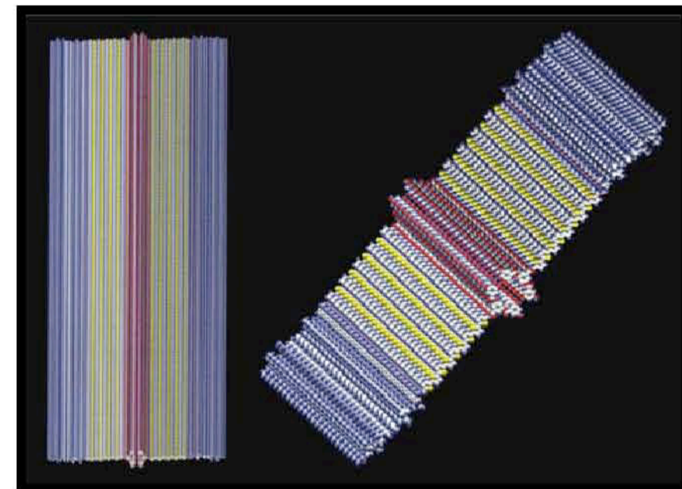
- Spontaneous organization of molecules into stable, structurally well-defined aggregates (nanometer length scale).
- Molecules can be transported to surfaces through liquids to form self-assembled monolayers (SAMs).



Supramolecular rodcoil "mushrooms"



Polythiophene wires



Supramolecular rodcoil nanoribbons

"Prediction is very difficult,

Especially of the future "

attributed to Niels Bohr

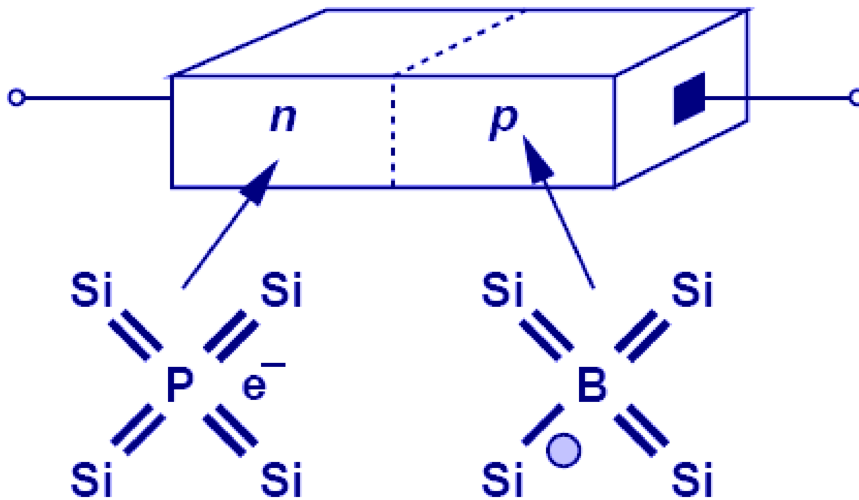
A quote to remember:

"The Federal Patent Office should be closed, because **everything** that can be invented has been invented."

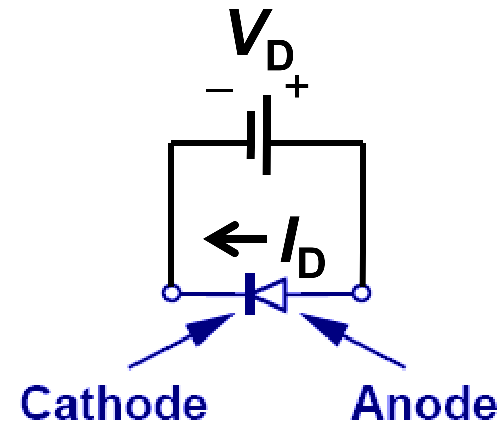
Charles Duell
Commissioner
Federal Office of Patents
1929

The PN Junction Diode

- When a P-type semiconductor region and an N-type semiconductor region are in contact, a PN junction diode is formed.



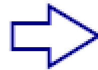
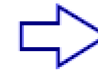
(a)



(b)

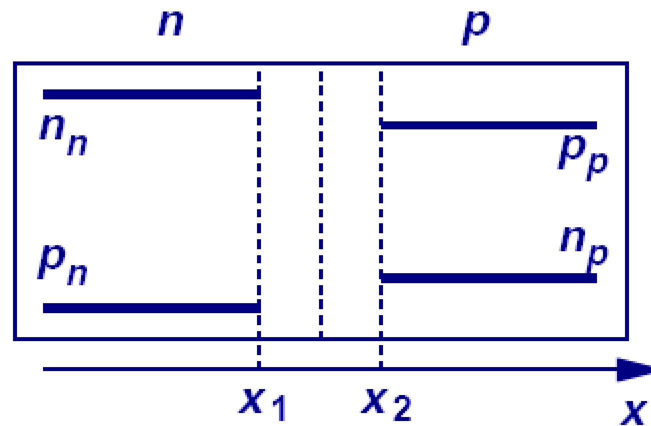
Diode Operating Regions

- In order to understand the operation of a diode, it is necessary to study its behavior in three operation regions: equilibrium, reverse bias, and forward bias.

$V_D = 0$		$V_D < 0$		$V_D > 0$
PN Junction in Equilibrium		**PN Junction Under Reverse Bias**		**PN Junction Under Forward Bias**
• Depletion Region • Built-in Potential		• Junction Capacitance		• I/V Characteristics

Carrier Diffusion across the Junction

- Because of the difference in hole and electron concentrations on each side of the junction, carriers diffuse across the junction:

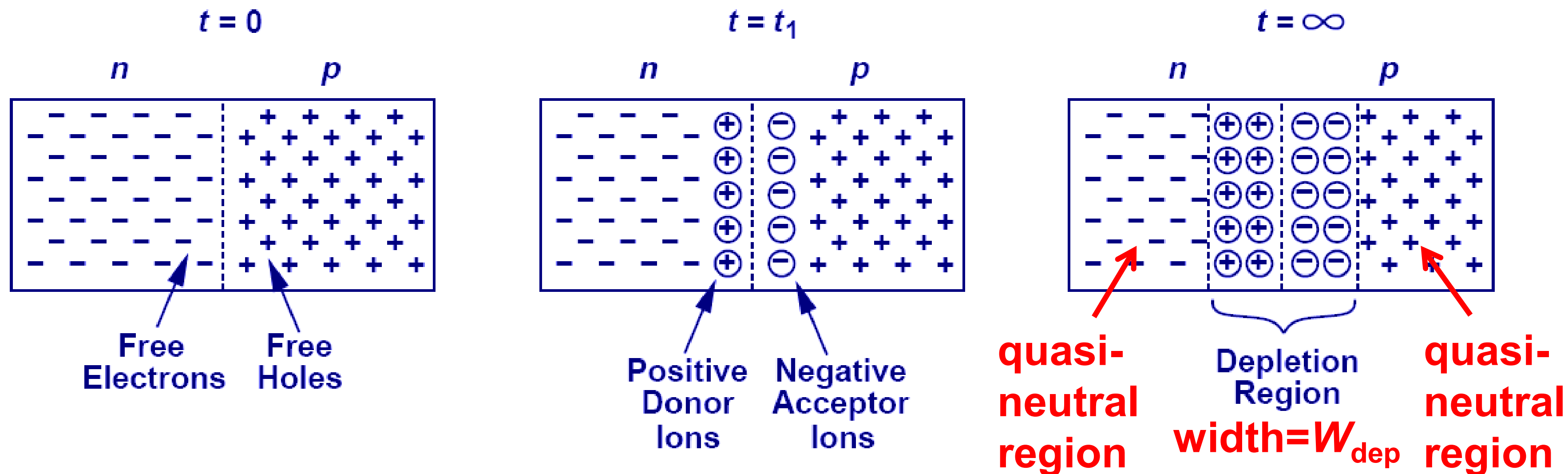


Notation:

$n_n \equiv$ electron concentration on N-type side (cm^{-3})
$p_n \equiv$ hole concentration on N-type side (cm^{-3})
$p_p \equiv$ hole concentration on P-type side (cm^{-3})
$n_p \equiv$ electron concentration on P-type side (cm^{-3})

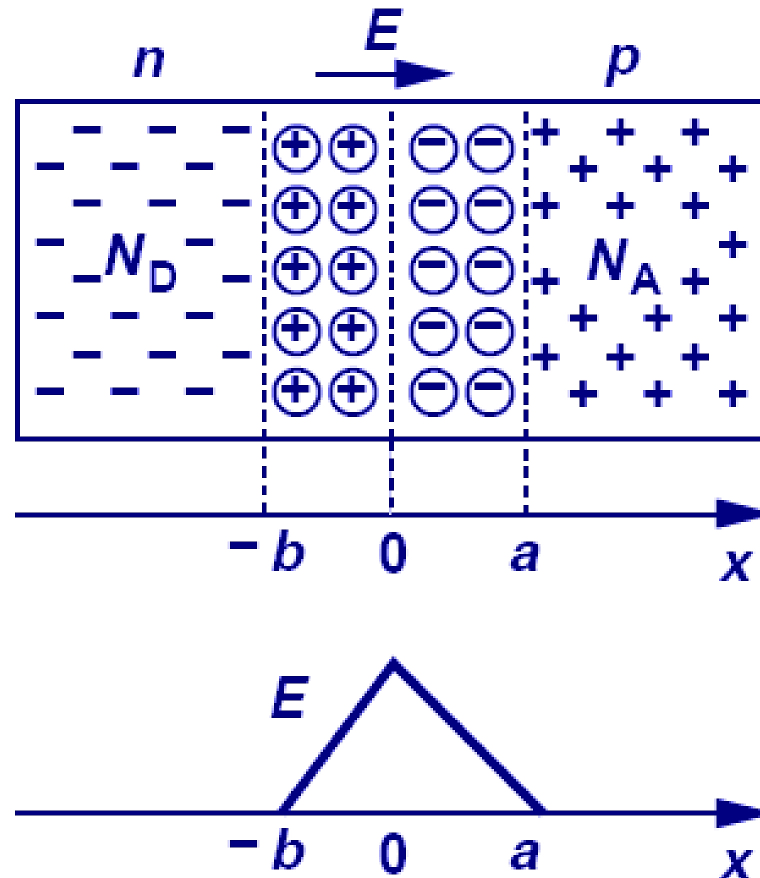
Depletion Region

- As conduction electrons and holes diffuse across the junction, they leave behind ionized dopants. Thus, a region that is depleted of mobile carriers is formed.
  - The charge density in the depletion region is not zero.
  - The carriers which diffuse across the junction recombine with majority carriers, *i.e.* they are annihilated.



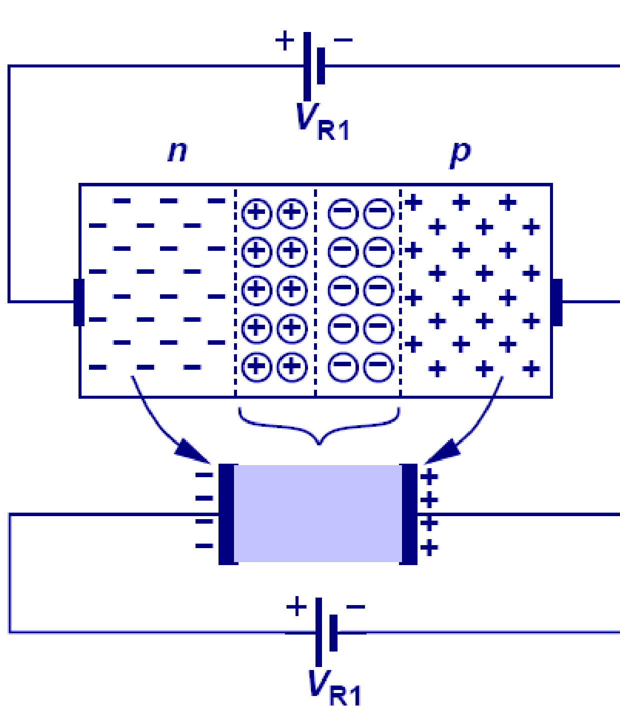
Carrier Drift across the Junction

- Because charge density ≠ 0 in the depletion region, an electric field exists, hence there is drift current.

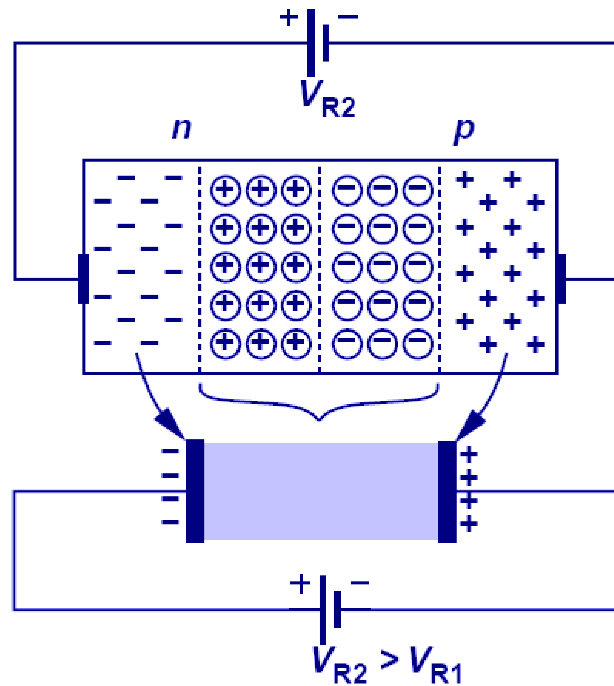


PN Junction Capacitance

- A reverse-biased PN junction can be viewed as a capacitor. The depletion width (W_{dep}) and hence the junction capacitance (C_j) varies with V_R.



(a)



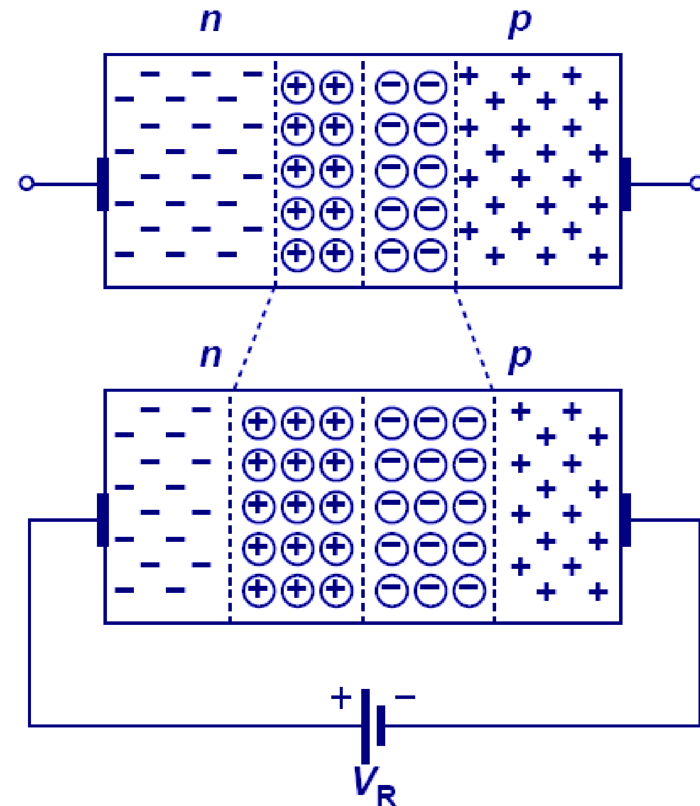
(b)

$$C_j = \frac{\varepsilon_{si}}{W_{dep}}$$

PN Junction under Reverse Bias

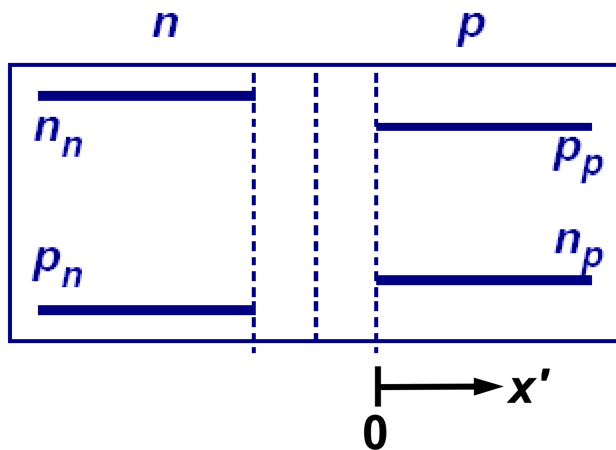
- A reverse bias increases the potential drop across the junction. As a result, the magnitude of the electric field increases and the width of the depletion region widens.

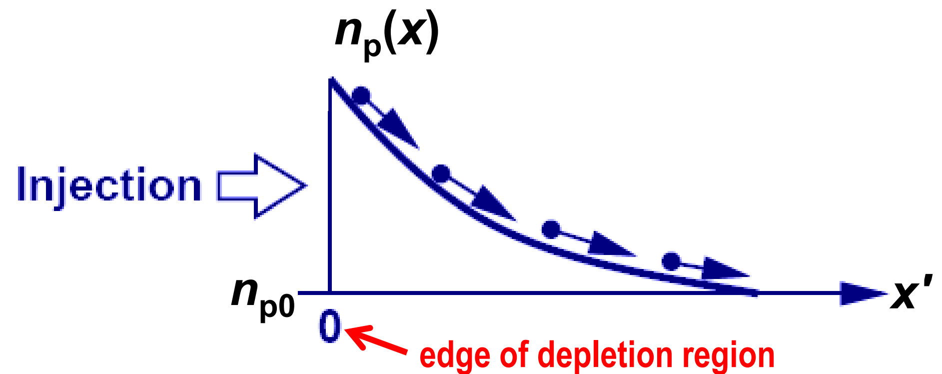
$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + V_R)}$$



Minority Carrier Injection under Forward Bias

- The potential barrier to carrier diffusion is decreased by a forward bias; thus, carriers diffuse across the junction.
  - The carriers which diffuse across the junction become minority carriers in the quasi-neutral regions; they recombine with majority carriers, "dying out" with distance.

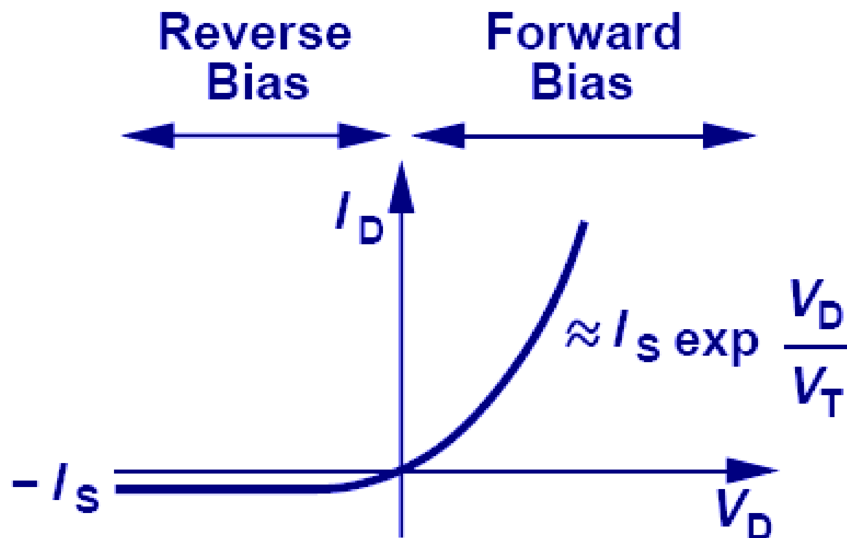




Equilibrium concentration of electrons on the P side: $n_{p0} = \frac{n_i^2}{N_A}$

I-V Characteristic of a PN Junction

- Current increases exponentially with applied forward bias voltage, and "saturates" at a relatively small negative current level for reverse bias voltages.



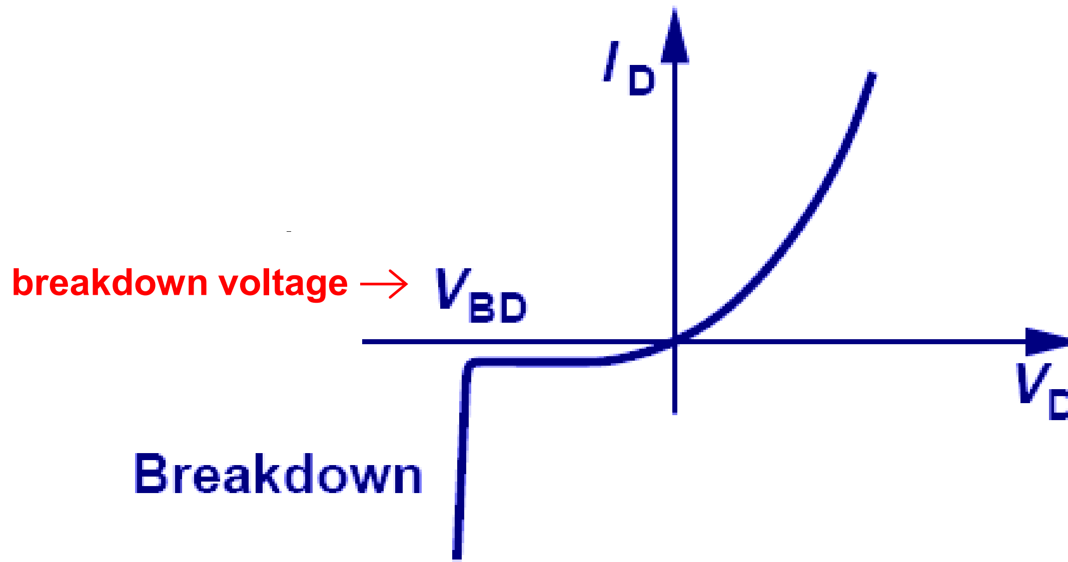
"Ideal diode" equation:

$$I_D = I_S\left(e^{V_D/V_T} - 1\right)$$

$$I_S = AJ_S = Aqn_i^2\left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right)$$

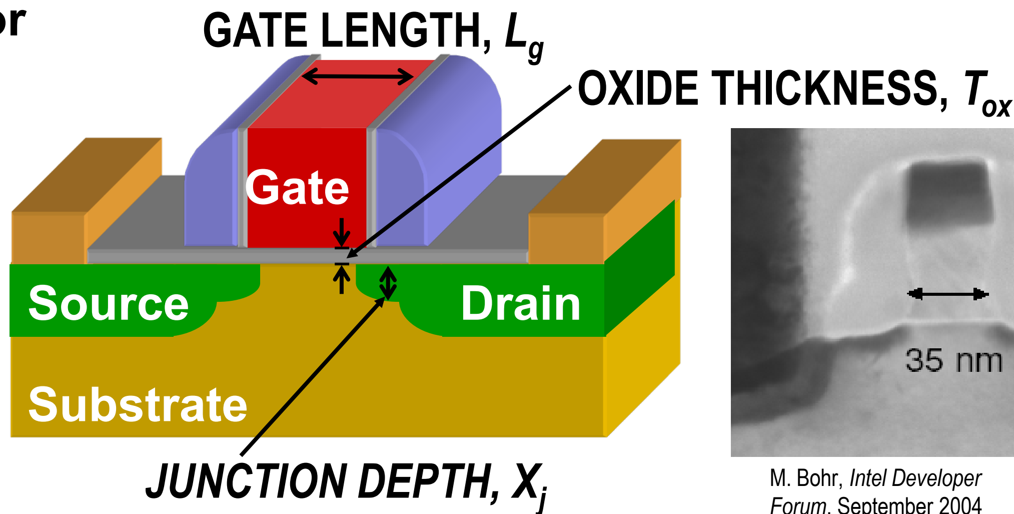
Reverse Breakdown

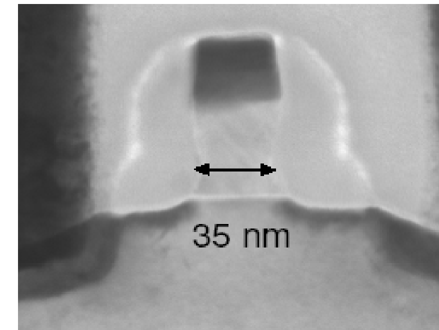
- As the reverse bias voltage increases, the electric field in the depletion region increases. Eventually, it can become large enough to cause the junction to break down so that a large reverse current flows:



The MOSFET

Metal-Oxide-Semiconductor Field-Effect Transistor:



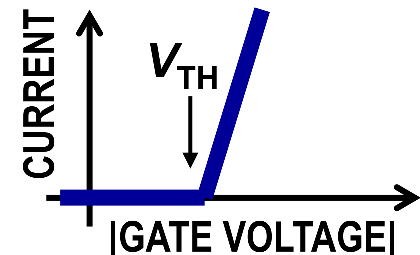


M. Bohr, *Intel Developer Forum*, September 2004

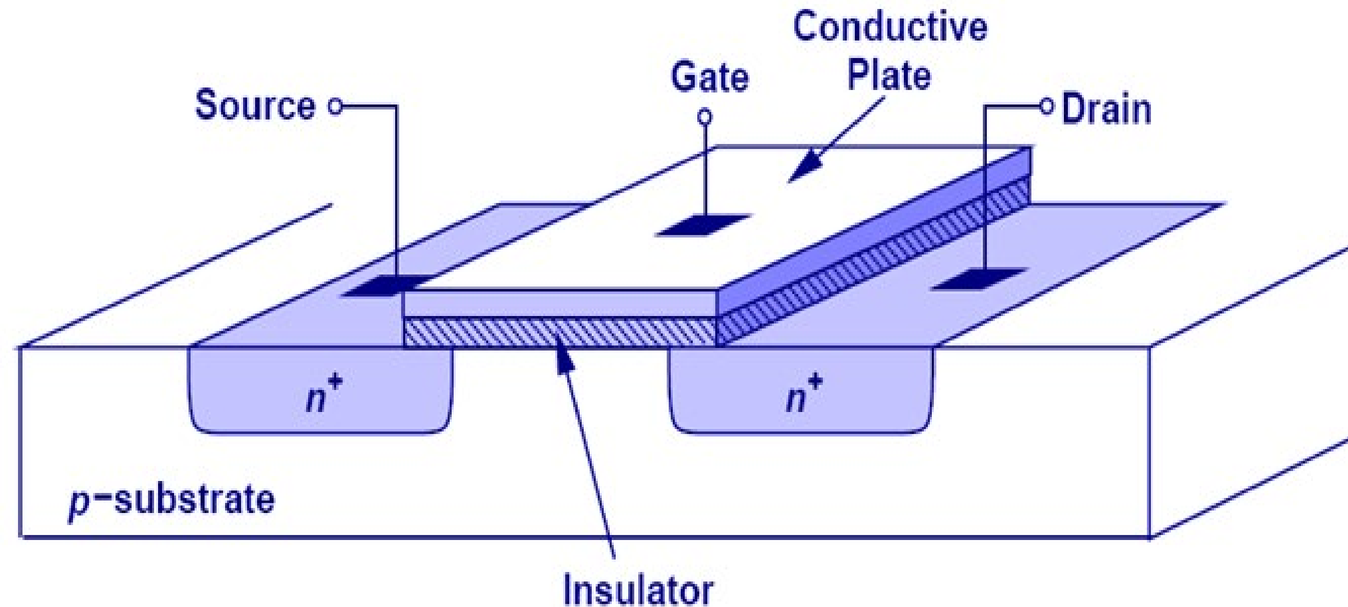
- Current flowing through the **channel** between the **source** and **drain** is controlled by the **gate** voltage.

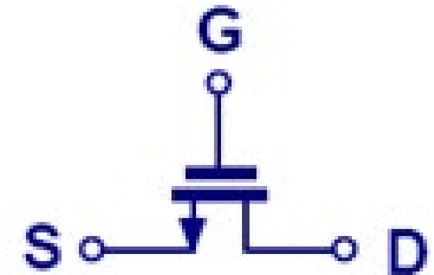
- **"N-channel" & "P-channel" MOSFETs operate in a complementary manner**

  "CMOS" = Complementary MOS



N-Channel MOSFET Structure

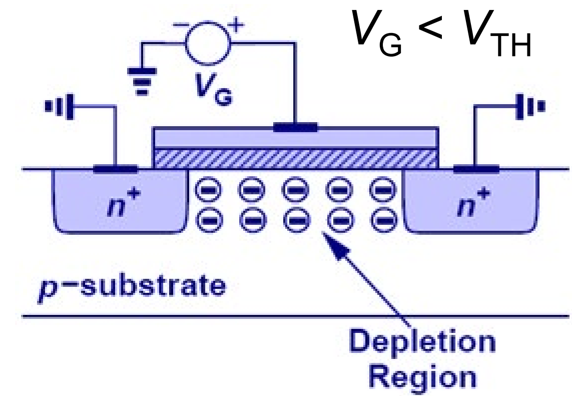




- The conventional gate material is heavily doped polycrystalline silicon (referred to as "polysilicon" or "poly-Si" or "poly")
  - Note that the gate is usually doped the same type as the source/drain, *i.e.* the gate and the substrate are of opposite types.
- The conventional gate insulator material is SiO_2.
- To minimize current flow between the substrate (or "body") and the source/drain regions, the p-type substrate is grounded.

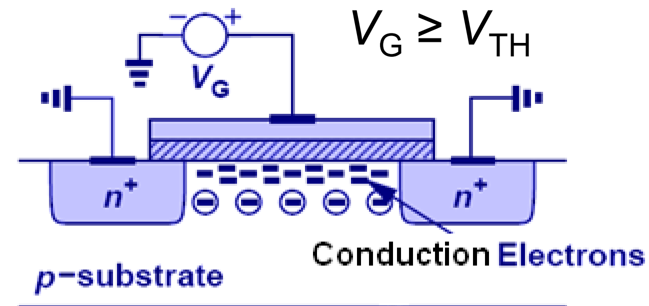
Channel Formation (Qualitative)

- As the gate voltage (V_G) is increased, holes are repelled away from the substrate surface.
  - The surface is depleted of mobile carriers. The charge density within the ***depletion region*** is determined by the dopant ion density.



- As V_G increases above the **threshold voltage** $\boldsymbol{V_{TH}}$**,** a layer of conduction electrons forms at the substrate surface.
  - For $V_G > V_{TH}$, $n > N_A$ at the surface.

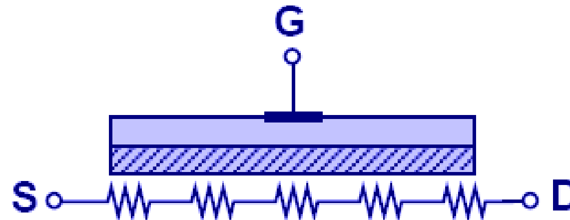
→ **The surface region is "inverted" to be n-type.**



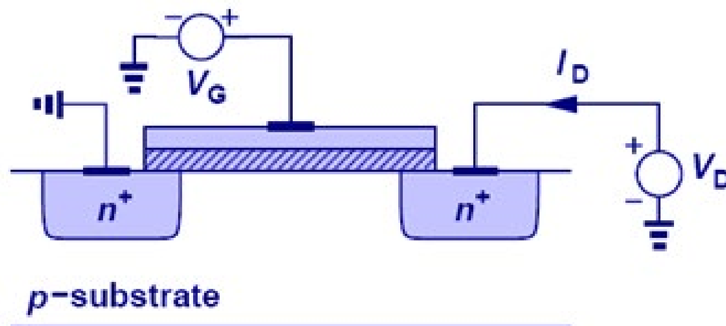
The electron ***inversion layer*** serves as a resistive path (***channel***) for current to flow between the heavily doped (*i.e.* highly conductive) ***source*** and ***drain*** regions.

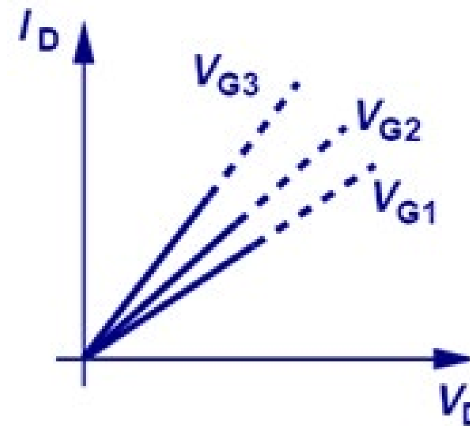
Voltage-Dependent Resistor

- In the ON state, the MOSFET channel can be viewed as a resistor.



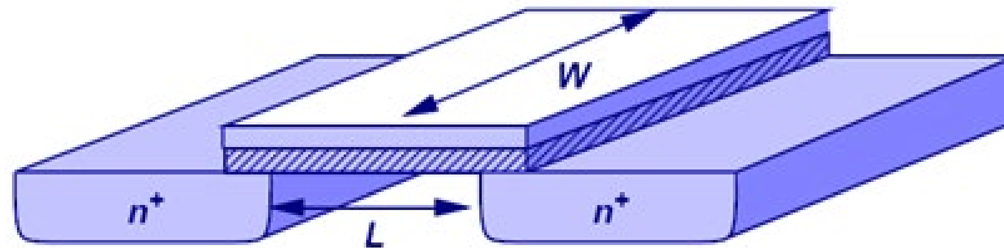
- Since the mobile charge density within the channel depends on the gate voltage, the channel resistance is voltage-dependent.

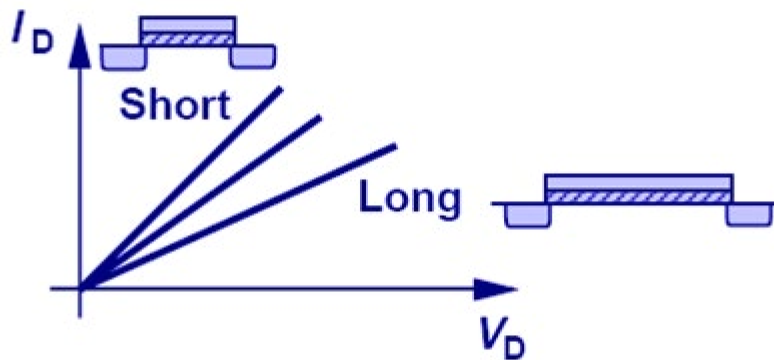


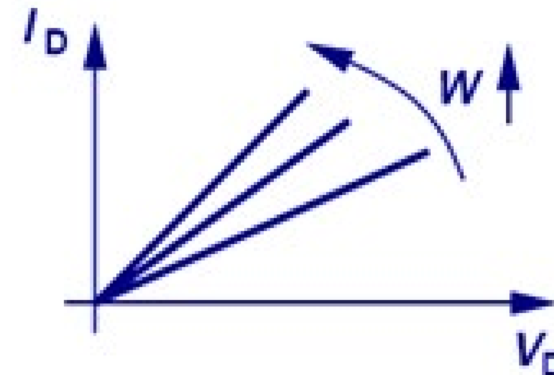


Channel Length & Width Dependence

- Shorter channel length and wider channel width each yield lower channel resistance, hence larger drain current.
  - Increasing *W* also increases the gate capacitance, however, which limits circuit operating speed (frequency).

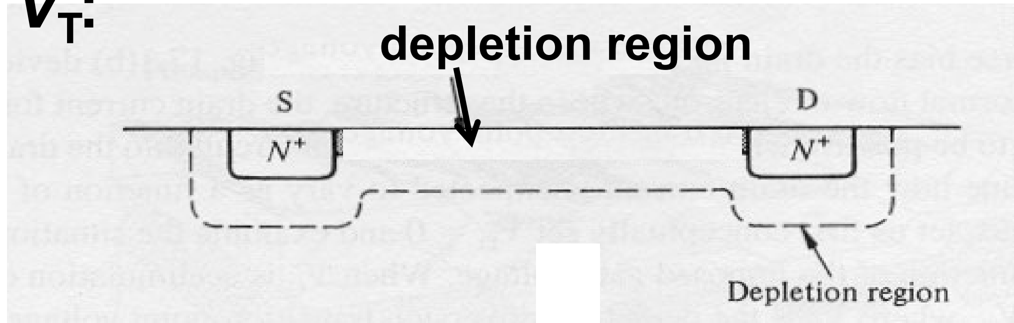






Charge in an N-Channel MOSFET

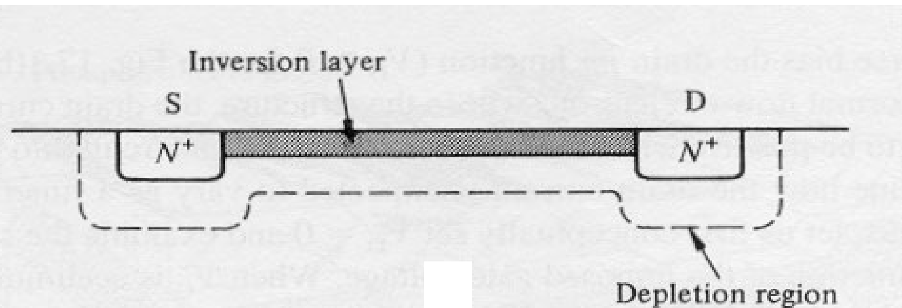
$V_{GS} < V_T$:



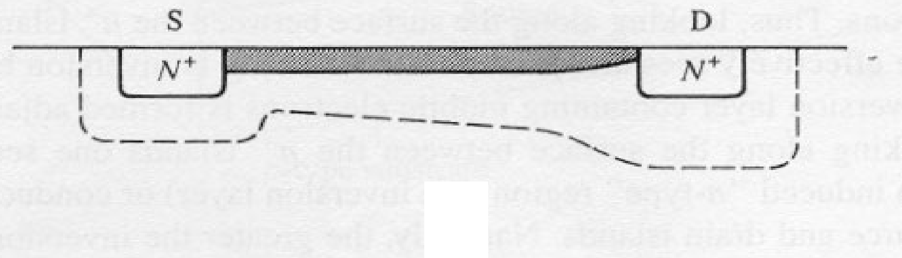
(no inversion layer at surface)

$V_{GS} > V_T$:

$V_{DS} \approx 0$



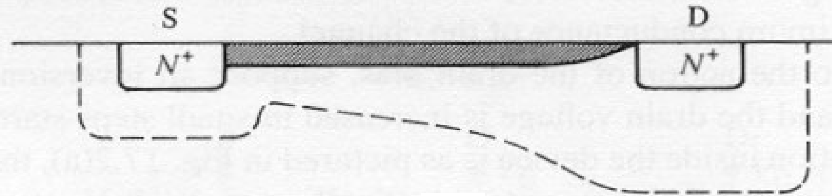
$V_{DS} > 0$ (small)



What Happens at Larger V_{DS}?

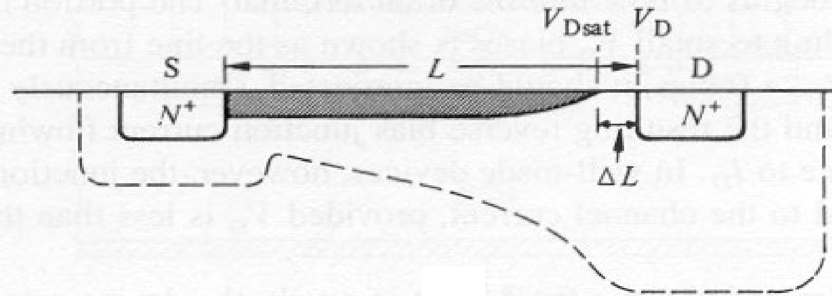
$V_{GS} > V_T$:

$V_{DS} = V_{GS} - V_T$



Inversion-layer is "pinched-off" at the drain end

$V_{DS} > V_{GS} - V_T$



As V_{DS} increases above $V_{GS} - V_T \equiv V_{DSAT}$, the length of the "pinch-off" region ΔL increases:

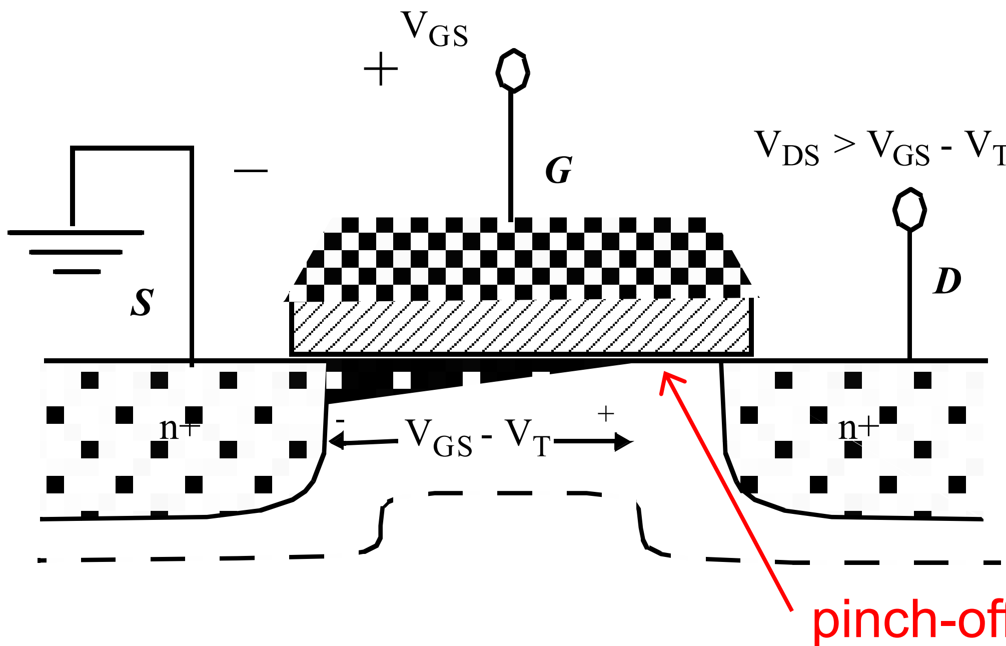
- **"extra" voltage ($V_{DS} - V_{Dsat}$) is dropped across the distance ΔL**
- **the voltage dropped across the inversion-layer "resistor" remains V_{Dsat}**

$\Rightarrow$ the drain current I_D saturates

Note: Electrons are swept into the drain by the *E*-field when they enter the pinch-off region.

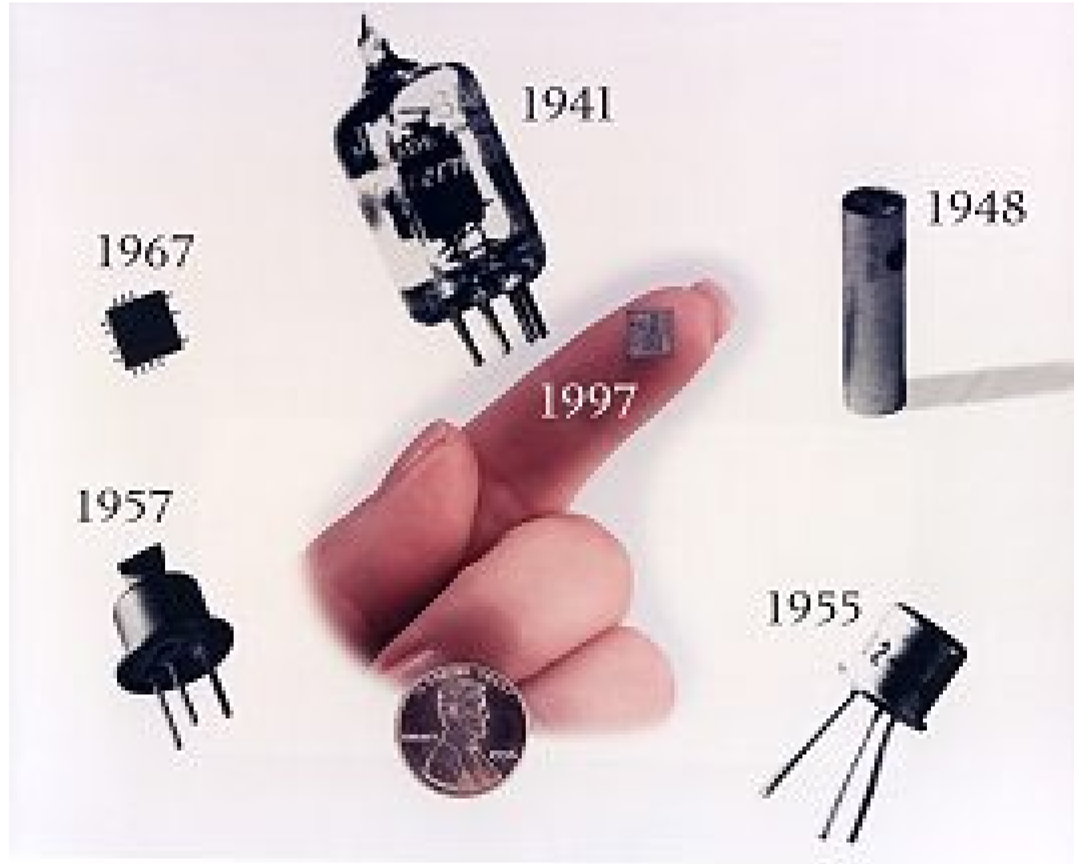
Summary of I_D vs. V_{DS}

- As V_{DS} increases, the inversion-layer charge density at the drain end of the channel is reduced; therefore, I_D does not increase linearly with V_{DS}.
- When V_{DS} reaches $V_{GS} - V_T$, the channel is "pinched off" at the drain end, and I_D saturates (*i.e.* it does not increase with further increases in V_{DS}).



$$I_{DSAT} = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2$$

Evolution of the Transistor



- The 1967 microchip contained two transistors and the 1997 microchip contained 5 million transistors!
- What technologies were used to put so many transistors?

Integrated Circuits

- Integrated Circuits (IC) were “invented” in 1958 by Jack Kilby at Texas Instruments & later Robert Noyce at Fairchild Semi.

Texas Instruments First IC
http://www.pbs.org/transistor/background1/events/icinv.html

- Idea was to build a transistor entirely on a silicon substrate in “one shot”

Czochalski Process

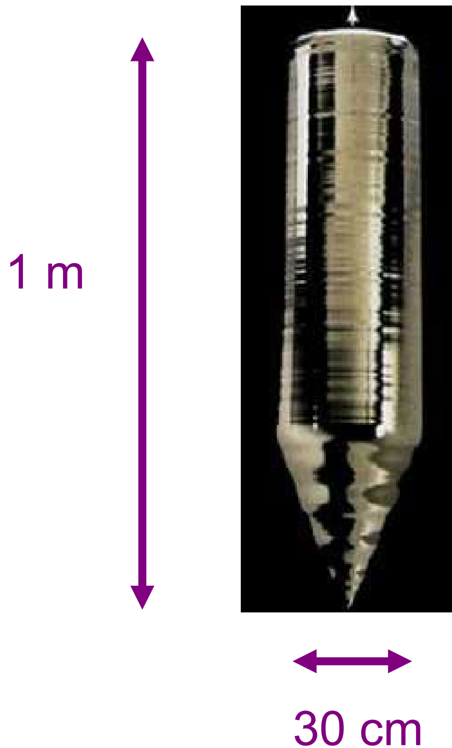
http://cnx.org/content/m1033/latest/

Argon Atmosphere
Seed
Puller Rod
Silicon Boule
Heater
Fused Silica Liner
Cool
Molten EGS
Temp-
erature
Grad-
ient
Hot

Technologies Involved in IC

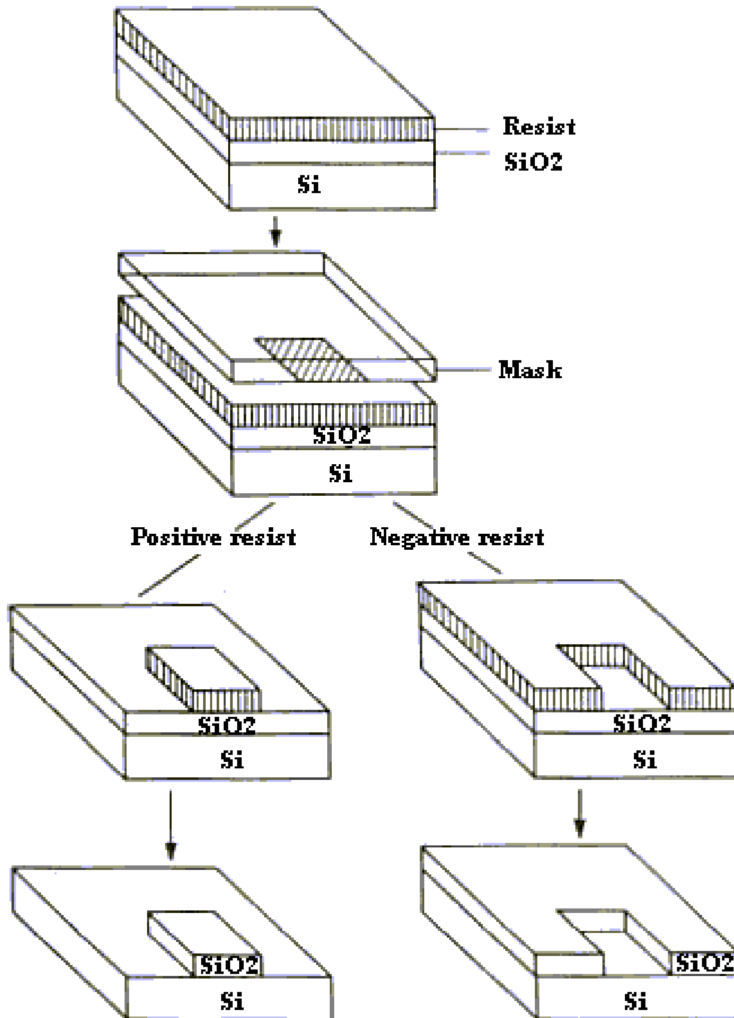
Looking at Just Silicon Technology

- Start with near-perfect single crystals of Si



- After boule is sliced, ***top-down lithography*** is performed

Top-Down: Photolithography



Step 1: Spin photoresist (a UV-sensitive polymer) and bake to cross link polymer

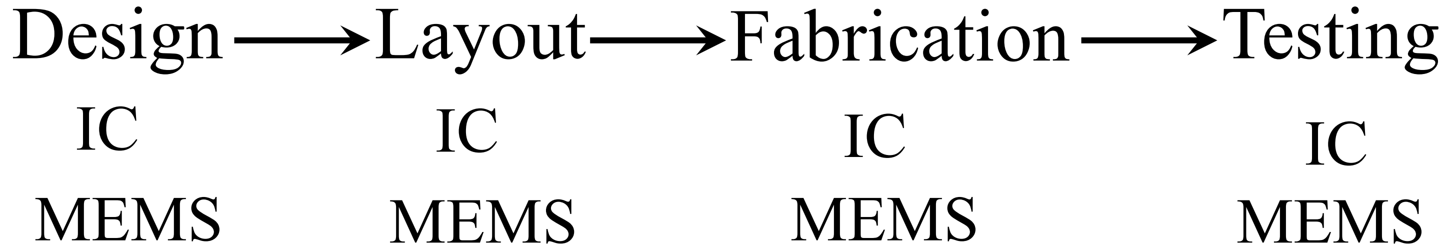
Step 2: UV expose to a mask—UV light will break cross-linked bonds

Step 3: Develop with developer

Step 4: Can then wet or dry etch

http://www.ece.gatech.edu/research/labs/vc/theory/photolith.html

Top-Down Fabrication



- Scale
  - 1μm = 10^{-6} m, Human hair ~ 100μm, Red blood cell ~ 5μm
  - State-of-art microelectronics – 45nm (Intel Processors)
- Clean room?
- About 2 billion dollars to build a 12-inch fab
  - Class 1 maximum number of 0.5μm particles/ft^3
  - Class 10 Typical IC fab
  - Class 100 Berkeley Microlab
  - ⋮
  - Class 1,000,000 Regular room

IC Process

- General fabrication flow
  - Wafer clean
  - Thin film deposition (SiO_2, Si_3N_4, metal …) ①
  - Lithography (mask#1, #2, …) ②
  - Etching ③